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The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Mechanical Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: DMX3572/MEX3272 – Applied electronics**
Academic Year	: 2017/18
Date	: 25th January 2019
Time	: 0930-1230hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Eight (8)** questions in **Seven (7)** pages.
3. Answer any **Five (5)** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
6. This is a Closed Book Test (CBT).
7. Answers should be in clear hand writing.
8. Do not use Red colour pen.

Q1.

(a) Write the equations needed to solve for the node voltages V_1, V_2, and V_3 in the circuit shown in Figure Q1-a. [06 marks]

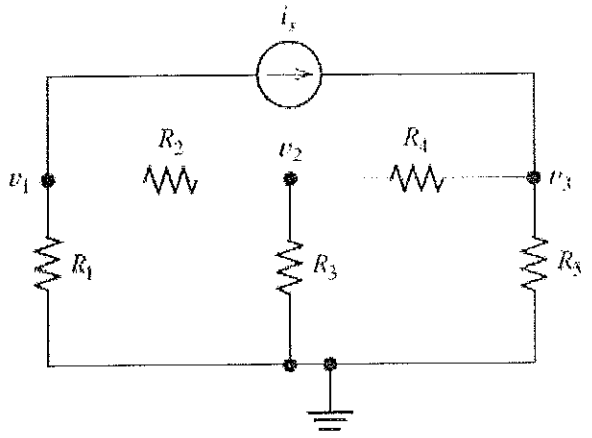

Figure Q1-a.

(b) Determine Thévenin and Norton equivalent circuits of the circuit illustrated in Figure Q1-b. [06 marks]

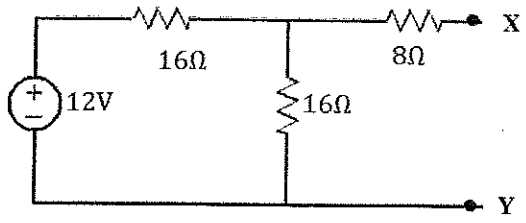

Figure Q1-b

(c) A Wheatstone bridge is illustrated in Figure Q1-d. *R*1 =12 k , *R*3 =240k , and *R*2 = 2k. If ig=0, determine *Rx*. [04 marks]

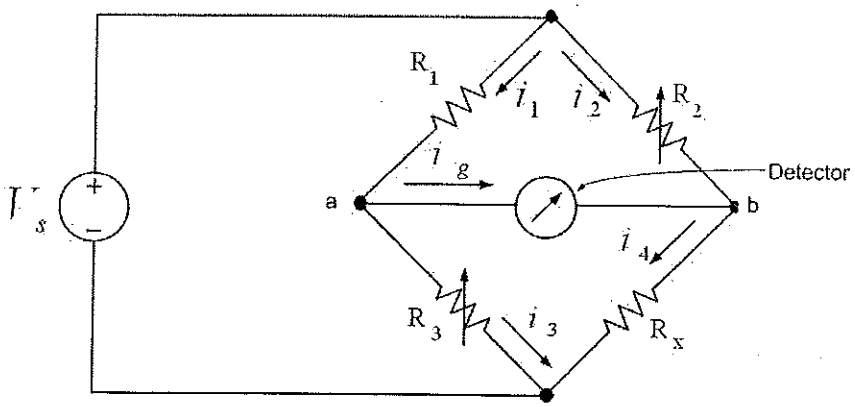

Figure Q1-d

(d) It is model a certain battery as a voltage source in series with a resistance. The open circuit voltage of the battery is 12V. When a 150Ω resistor is placed across the terminals of the battery, the voltage drops to 9V. Find the Thevenin resistance (internal resistance) of the battery. [04 marks]

Q2.

(a) A double diode clipper circuit shown in Figure Q2-a can be used to limit the peaks of both half cycles of the 10V AC input signal. Sketch the output signal (You should indicate the magnitudes of the signal). [06 marks]

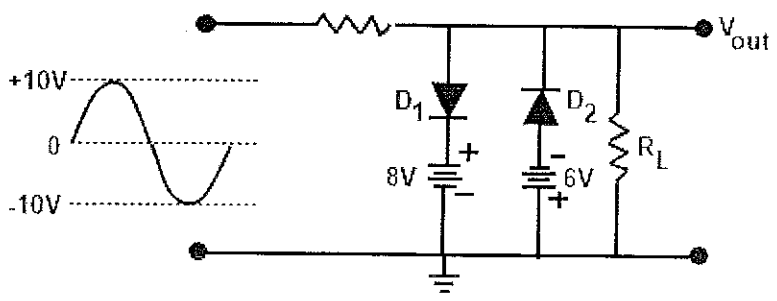

Figure Q2-a

(b) A Zener circuit shown in figure Q2-b. Given that $v_i = 10sin\omega t$, $V_{z1} = V_{z2} = 5V$, explain the operation of the circuit and sketch the V_o waveform. Assume that both zener diodes have a voltage drop of 0.7V when forward bias. [06 marks]

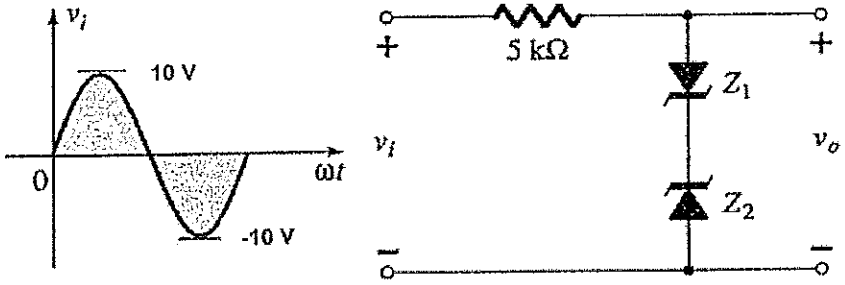

Figure Q2-b

(c) Explain the functions of following diode types. [04 marks]

i. Varactor diodes

ii. Catch diode (freewheeling diode)

(d) Briefly explain any two applications of FET. [04 marks]

Q3.

(a) Briefly explain the function of any four types of filter circuits. [04 marks]

(b) A simple Amplifier system is shown in figure Q3 –b.

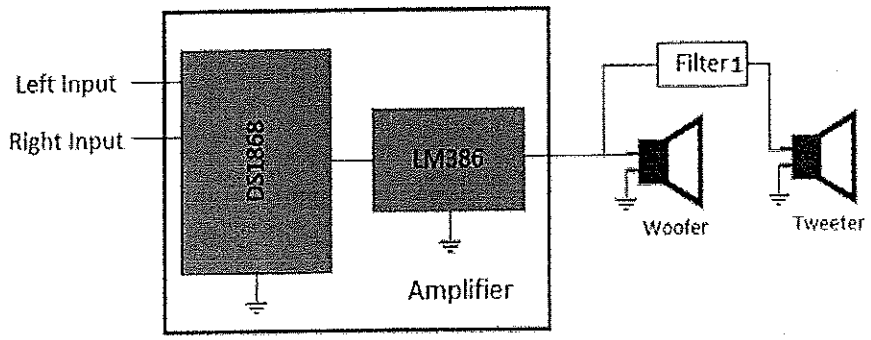

Figure Q3–b

i) Suggest a suitable filter circuit for the Filter-1 and justify your suggestion. [03 marks]

ii) Now, you want to add another filter to the woofer. Suggest a most suitable filter for the woofer and give reasons. [03 marks]

(c) Suppose that R = 5000 Ω and C = 1 μF in the circuit of figure Q3-c. The capacitor charged to V_i prior to t=0. Find the time at which the voltage across the capacitor reaches 36.8% of its initial value (V_i). [05 marks]

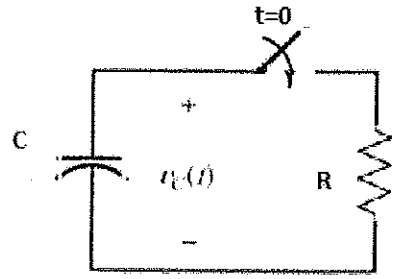

Figure Q3–c

(d) Find v_x and i_x for the circuit shown in figure Q3-d for t »0 (After the switch has been closed for a long time, we expect the transient response to have decayed to zero. Then the circuit is operating in dc steady-state conditions). [05 marks]

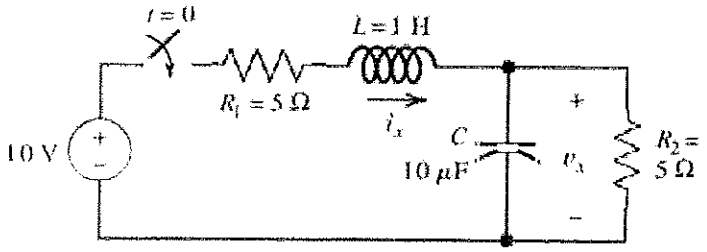

Figure Q3–d

Q4.

(a) A dc bias circuit is shown in Figure Q4 has R_B = 200 k , R_C = 1k , and V_{CC} = 15V. Gain of The transistor is 100. Determine I_C and V_{CE}. [06 marks]

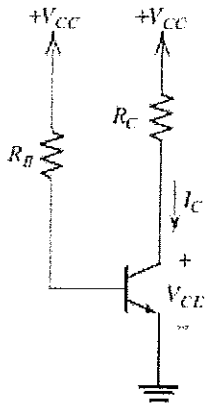

Figure Q4-a

(b) Draw the output load line for the circuit shown in Figure Q4-b , If Vcc= 10V and Rc= 2k. Repeat for Vcc= 15V. [06 marks]

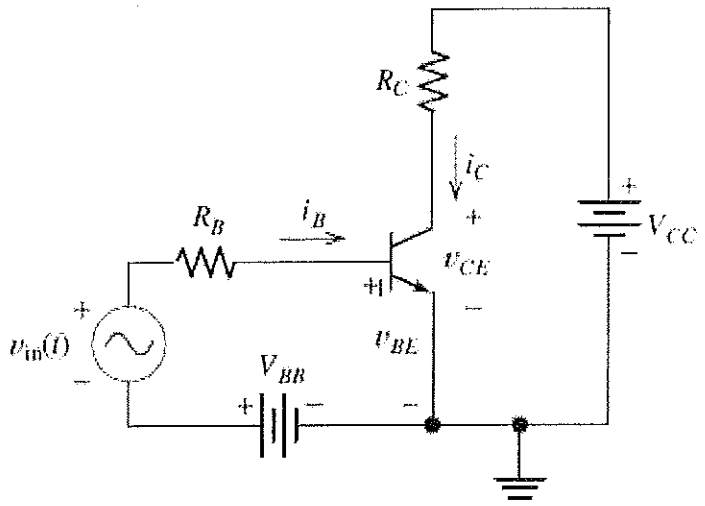

Figure Q4-b

(c) The dc current gain of the transistor of the circuit shown in Figure Q4-c is 100. V_{CE} =8V, R_B = 360 k and R_C = 2k. Determine Q point and draw the dc load line. [08 marks]

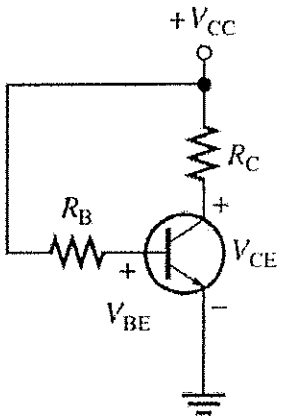

Figure Q4-c

Q5.

(a) What are the characteristics of an ideal op-amp? List any three characteristics. [03 marks]

(b) Name any real op amp IC known by you. Name the probable function for at least five terminals of the IC. [03 marks]

(c) Determine the Vo of the operational amplifier shown in Figure Q5-c. V_1=2V, V_2= 1V, R_1= 10k, R_2=5k. [05 marks]

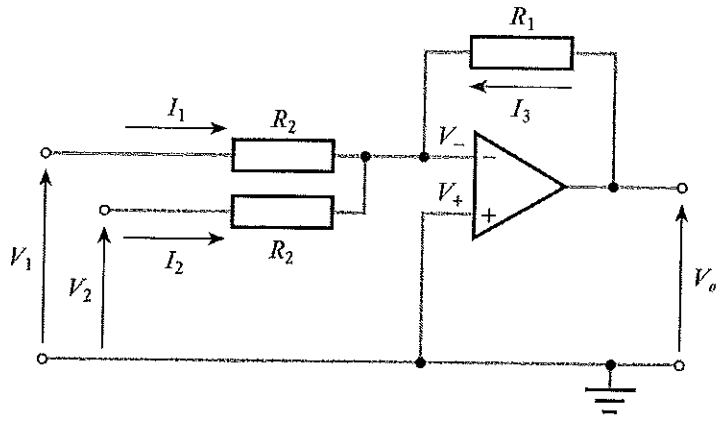

Figure Q5-b

(d) Determine the Vout of the operational amplifier shown in Figure Q5-d. V_{in}=2V, R_1= 10k, R_2=5k. [5 marks]

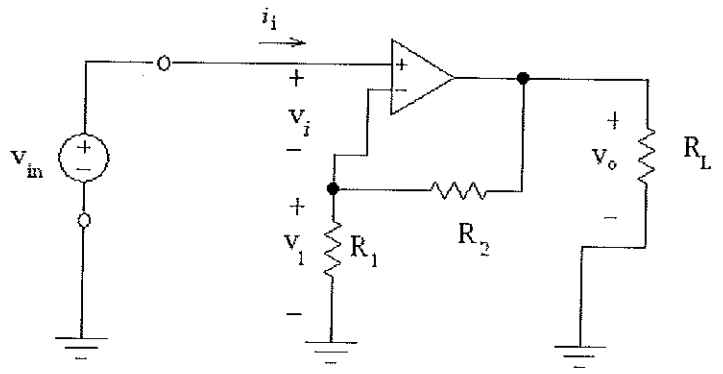

Figure Q5-d

(e) A differential amplifier with a voltage gain of 50 has a common input signal of 2V to both terminals. This results in an output signal of 20 mV. Determine the common-mode gain and the CMRR. [4 marks]

Q6.

(a) Perform the following conversions between number systems with clearly showing the necessary steps.

i) 16.2_8 to decimal, binary and hexa-decimal

ii) 1100.1_2 to decimal and octal

[05 marks]

(b) Two's complement representation of an 8 bit binary number is given as 11111010. Determine the decimal value of the number. [03 marks]

(c) Sign magnitude representation of an 8 bit binary number is given as 10000101. Determine the decimal value of the number. [03 marks]

(d) Determine one's complement (8 bit) representations of the -16_{10}. [03 marks]

(e) Briefly explain the operation of the half adder circuit. Draw the logic circuit of it.

[06 marks]

Q7.

(a) Rewrite the following Boolean expression using De-Morgan's theorem and implement the logic circuit using **NAND** gates only. [4 marks]

$$Q = \overline{X + Y}$$

(b) Simplify the following Boolean expression using Boolean Theorems. [4 marks]

i. A+AB
ii. $A + \bar{A}$
iii. $\bar{\bar{A}} + A$
iv. (A+1) • (A•A)

(c) Simplify the following Boolean function using K-maps.

f (A, B, C, D) = Σm (0, 2, 3, 4, 5, 7, 9, 13, 15)

[4 marks]

(d) Determine the minimal sum of product (SOP) and minimal product of sums (POS) of the following Boolean expression using k-maps.

f (A, B, C, D) = Σm (1, 2, 3, 5, 6, 7, 8, 13) [4 marks]

(e) What are the universal gates? Briefly explain. [4 marks]

Q8.

(a) Draw a circuit diagram of a SR latch and explain the operation. [5 marks]

(b) Complete the corresponding timing diagram of the circuit shown in figure Q8-b

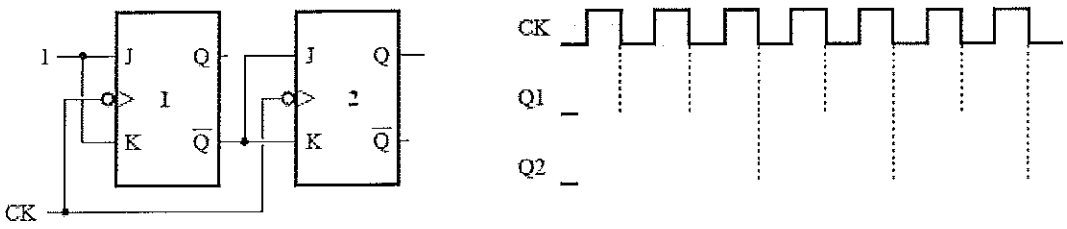

Figure Q8-a

[5 marks]

(c) Design a counter to count in the following sequence: 0, 1, 2, 3, 4, 5, 6, and 7. Use JK flip-flops and logic gates. Show the state transition diagram, present state-next state table, K-map, logic expressions and the circuit implementation clearly.

[10 marks]

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