The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX5536/ECX5236 Computer architecture**
Academic Year	: 2017/18
Date	: 2nd February 2019
Time	: 0930-1230hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Eight (8)** questions in **Four (4)** pages.
3. Answer any **Five (5)** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. This is a Closed Book Test (CBT).
6. Answers should be in clear hand writing.
7. Do not use Red colour pen.

1. A design of an instruction execution path has L logic delays. So it will take L time to execute an instruction in one-stage pipeline. However the logic path can be divided into a number of stages. In the multistage pipeline it is assume that logic delay L is equally subdivided. Accordingly in each stage the minimum clock period is calculated as $T_{clock} = t_{max} + \tau$; where t_{max} is approximated to the largest delay of a stage and τ is the sum of setup time of a latch and clock skew. Let k as the length of the instruction sequence and s as the number of stages.

   (i) What is the minimum clock period T_{clock} in terms of $\boldsymbol{L, s}$ and $\boldsymbol{\tau}$?

   (ii) What is the execution time of the $\boldsymbol{k}$ number of instructions?

   (iii) Derive an equation to calculate the optimum number of stages in the pipeline?

   (iv) Prove the minimum execution time of $\boldsymbol{k}$ number of instructions is $(\sqrt{\boldsymbol{L}} + \sqrt{\boldsymbol{\tau(k-1)}})^2$

2. An enhancement in a computer system improves only some part of the system. Accordingly, improvement of the performance depends on the impact of the enhancement part. The f denotes the fraction of the computational time in the old system that can be improved with the enhancement mad; S_e is the achievable speedup only if the enhanced part of the system is used.

   (i) If the old time of the system (without improvement) is T_{old} formulate the new time T_{new} of the system after the enhancement.

   (ii) The speedup of the new system (after the improvement) is

   $$S_{new} = \frac{T_{old}}{T_{new}}$$

   Accordingly derive an equation for S_{new} in terms of f, S_e, which is Amdahl's law.

   (iii) Implementations of floating-point (FP) square root vary significantly in performance. Suppose FP square root is responsible for 20% of the execution time of a critical benchmark on a machine. One proposal is to add FP square root hardware that will speed up this operation by a factor of 10. The other alternative is just to try to make all FP instructions run faster; FP instructions are responsible for a total of 50% of the execution time. The design team believes that they can make all FP instructions run two times faster with the same effort as required for the fast square root.

   a. Compare these two design alternatives giving all calculations.

   b. What percentage of the FP instructions' execution time would make the hardware solution better?

3. Specification of a hard disk of 1.2 GB made up with several platters is given as follows: 620 cylinders, 64 heads, and 63 sectors. The performance measuring utility shows the average seek time as 9ms. Disk rotational speed is calculated as 3600 rpm.

   (i) Define the terms seek time and rotational delay.
   (ii) Calculate the number of bytes in a sector of the hard disk. (Note: bytes in a sector should be the nearest to the power of two value)
   (iii) Calculate the average rotational delay.
   (iv) How many tracks are there in a cylinder of the disk?
   (v) Calculate how many tracks are needed to store a file in size of 3 MB?
   (vi) What would be the approximate time taken to read a file in size of 3 MB? (Note: assume the file is continuously stored from the 0^{th} sector of the 0^{th} track of any cylinder and the data transfer rate as 1890 kB/s). Consider that the arm may not be positioned on the cylinder where the file is stored before starting to read the file.)
   (vii) How many files in size of 3 MB can be saved on that disk?

4.
   (i) Draw typical virtual machine schematics for different styles of Instruction Set Architecture (ISA) i.e. Accumulator, Memory-Memory, Stack, Load-Store.
   (ii) Identify the general purpose and special purpose registers in each of the architectures mentioned above.
   (iii) What are the addressing modes of the following Intel 8086 instructions?

   (a) MOV AL, BL ; (AL) ← (BL)

   (b) ADD AL, data ; (AL) ← (AL) + data

   (c) AND AX, addr ; (AX) ← (AX) AND (addr)

   Note: AL, AX and BL belong to the register set. Here addr is an address of a memory location and data is a data value.

5. A hierarchical Cache – primary memory subsystem has following specifications: cache access time of 50ns, main storage access time of 500ns, 80% of memory request are for read, hit ratio of 0.9 for read access and the Write Through policy is employed. Estimate the following.
   (i) Average access time of the system considering only the memory read cycle.
   (ii) Average access time of the system both for read and write requests.
   (iii) The hit ratio taking into consideration the write cycle.

6. A computer is constructed using a 3.6 GHz processor. It is integrated with 512 MB RAM which has 1.5 ns latency. The processor has 3 types of instructions: Branch, Arithmetic & Logic, and Memory Move. The processor needs 5, 4, and 5 clocks to execute each type of instructions respectively. It is observed that of all the instructions executed 20% are Branch instructions and 40% are Arithmetic and Logic operations. Branch and Memory Move instructions need 2 memory access but Arithmetic and Logic instructions need only one.

   (i) Calculate the average CPI of the processor.
   (ii) Find the MIPS rating of the processor.
   (iii) Calculate the MIPS rating of the computer.
   (iv) Estimate the time taken to execute a program with n number of instructions.

7. You are asked to design a simple CPU with the following specifications. Only 256 Kbytes of address space are needed. In order to make the CPU as simple as possible it has been restricted to 16 instructions with 2 different addressing modes. You have the option of deciding the number of registers in the CPU.

   (i) How many registers would you suggest for the design? Explain.
   (ii) Draw a suitable instruction format for your design.
   (iii) What addressing modes do you select for instructions? Give reasons for your selection.
   (iv) Draw a complete architecture of your design. You have to show the data path and the memory interfaced with the CPU.

8.
   (i) Describe the Flynn's classification on computer organization giving block diagrams for each organization.
   (ii) Distinguish MIMD multiprocessors from multi-computers or computer networks.
   (iii) What are the salient features of RISC architecture and CISC architecture? Provide advantages and disadvantages of each architecture.
   (iv) A transaction processing system is considered for a PC. The PC executes instructions at 100 MIPS and has a disk with a total mean access time of 20 *ms*. Four disk accesses and 100,000 instructions are needed for each transaction. How many transactions per second are possible with the system?

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