The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering

00045

Study Programme	: Bachelor of Software Engineering Honours
Name of the Examination	: Final Examination
Course Code and Title	**: EEX5563/ECX5263 Computer Organization and Operating Systems**
Academic Year	: 2017/2018
Date	: 02nd February 2019
Time	: 0930-1230hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Eight (8)** questions in **Five (5)** pages.
3. Answer any **Five (5)** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. Relevant charts/ codes are provided.
6. This is a Closed Book Test (CBT).
7. Answers should be in clear handwriting.
8. Do not use Red colour pen.

1. Consider the given set of actions in the following Table Q1. "P" indicates a process and "R" indicates a resource.

Table Q1: Set of actions against the time of arrival

Time	Action
1	P1 requests R2 and R1 is allocated to P1
2	P2 requests R1
3	P2 requests R2
4	P3 requests R2
5	P3 requests R3, R3 and R4 are allocated to P3
6	P4 requests R3 and R4

i) Draw a resource allocation graph to analyze the above scenario. State if any assumptions.

[08 Marks]

ii) Is there a deadlock in the above system? Justify your answer.

[06 Marks]

iii) Describe "race condition" and "starvation" by giving appropriate examples.

[06 Marks]

2. Consider the set of processes, with the arrival time and the length of the CPU burst time given in seconds in the Table Q2.

Table Q2: Processes against the process arrival time and the CPU burst time

Process	Arrival Time (hh:mm:ss)	CPU Burst Time (s)
P_0	00:00:00	1
P_1	00:00:01	2
P_2	00:00:02	1
P_3	00:00:03	3
P_4	00:00:08	2
P_5	00:00:11	5
P_6	00:00:13	5

i) Draw four (4) Gantt charts that illustrate the execution of these processes using the following algorithms:

   a) First Come First Served(FCFS)
   b) Shortest Job First(SJF)
   c) Shortest Remaining Time First(SRTF)
   d) Round Robin(RR) algorithms. Choose the proper quantum size for RR scheduling and clearly state the reasons to select the quantum size. State assumptions clearly if any.

[10 Marks]

ii) Calculate the following if the Round Robin algorithm was used.
   a) the average turnaround time
   b) the average waiting time
   c) throughput

[03 Marks]

iii) Illustrate how the states of the process P3 change from state to state, from the creation to termination of the process using a process transition diagram.

[07 Marks]

3. Design of an instruction execution path has L logic delays. Therefore, it will take L time to execute an instruction in one-stage pipeline. However, the logic path can be divided into a number of stages. In the multistage pipeline, it is assumed that logic delay L is equally subdivided. Accordingly, in each stage, the minimum clock period is calculated as $T_{clock} = t_{max} + \tau$; where t_{max} is approximated to the largest delay of a stage and τ is the sum of setup time of a latch and clock skew. Let k as the length of the instruction sequence and s as the number of stages.

   (i) What is the clock period T_{clock} in terms of $\boldsymbol{L}, \boldsymbol{s}$ and $\boldsymbol{\tau}$?

   [03 Marks]

   (ii) What is the execution time of the $\boldsymbol{k}$ number of instructions?

   [05 Marks]

   (iii) Derive an equation to calculate the optimum number of stages in the pipeline?

   [06 Marks]

   (iv) Prove the minimum execution time of the $\boldsymbol{k}$ number of instructions is $(\sqrt{\boldsymbol{L}} + \sqrt{\boldsymbol{\tau(k-1)}})^2$

   [06 Marks]

4. An enhancement in a computer system improves only some part of the system. Accordingly, improvement of the performance depends on the impact of the enhancement part. The f denotes the fraction of the computational time in the old system that can be improved with the enhancement made; S_e is the achievable speedup only if the enhanced part of the system is used.

   (i) If the old time of the system (without improvement) is T_{old} formulate the new time T_{new} of the system after the enhancement.

   [03 Marks]

   (ii) The speedup of the new system (after the improvement) is

   $$S_{new} = \frac{T_{old}}{T_{new}}$$

   Accordingly derive an equation for S_{new} in terms of f, S_e, which is Amdahl's law.

   [05 Marks]

   (iii) Implementations of floating-point (FP) square root vary significantly in performance. Suppose FP square root is responsible for 20% of the execution time of a critical benchmark on a machine. One proposal is to add FP square root hardware that will speed up this operation by a factor of 10. The other alternative is just to try to make all FP instructions run faster; FP instructions are responsible for a total of 50% of the execution time. The design team believes that they can make all FP instructions run two times faster with the same effort as required for the fast square root.

      a. Compare these two design alternatives giving all calculations.

      [06 Marks]

      b. What percentage of the FP instructions' execution time would make the hardware solution better?

      [06 Marks]

5. Specification of a hard disk of 1.2 GB made up with several platters is given as follows: 620 cylinders, 64 heads, and 63 sectors. The performance measuring utility shows the average seek time as 9ms. Disk rotational speed is calculated as 3600 rpm.

   (i) Define the terms seek time and rotational delay.

   [02 Marks]

   (ii) Calculate the number of bytes in a sector of the hard disk. (Note: bytes in a sector should be the nearest to the power of two value)

   [02 Marks]

   (iii) Calculate the average rotational delay.

   [02 Marks]

   (iv) How many tracks are there in a cylinder of the disk?

   [01 Marks]

   (v) Calculate how many tracks are needed to store a file in size of 3 MB?

   [04 Marks]

   (vi) What would be the approximate time taken to read a file in size of 3 MB? (Note: assume the file is continuously stored from the 0^{th} sector of the 0^{th} track of any cylinder and the data transfer rate as 1890 kB/s). Consider that the arm may not be positioned on the cylinder where the file is stored before starting to read the file.)

   [05 Marks]

   (vii) How many files in size of 3 MB can be saved on that disk?

   [04 Marks]

6. A computer is constructed using a 3.6 GHz processor. It is integrated with 512 MB RAM which has 1.5 ns latency. The processor has 3 types of instructions: Branch, Arithmetic & Logic, and Memory Move. The processor needs 5, 4, and 5 clocks to execute each type of instructions respectively. It is observed that of all the instructions executed 20% are Branch instructions and 40% are Arithmetic and Logic operations. Branch and Memory Move instructions need 2 memory access but Arithmetic and Logic instructions need only one.

   (i) Calculate the average CPI of the processor.

   [02 Marks]

   (ii) Find the MIPS rating of the processor.

   [05 Marks]

   (iii) Calculate the MIPS rating of the computer.

   [08 Marks]

   (iv) Estimate the time taken to execute a program with n number of instructions.

   [05 Marks]

7.

(i) Write an algorithm in pseudo-code to deallocate memory blocks for dynamic partition memory allocation system.

[08 Marks]

(ii) Consider the Page Map Table(PMT) given as Table Q7.

Table Q7: Page Map Table

Page No.	Page Frame Number
0	5
1	3
2	7
3	1

If the page frame size in main memory is set to 512 bytes and the page size is 512 bytes, in "Page Memory Allocation", explain how the 1032nd line, which is to be loaded next, is found. Assume it takes 1 byte to store one line of code. State any assumptions.

[06 Marks]

(iii) Compare the following;

a) Internal fragmentation and external fragmentation
b) Virtual memory with paging and segmentation

[06 Marks]

8. Write the most appropriate short answer (word or phrase) for the following questions in your answer script. It is NOT required to attach the question paper.

(i) _____ is an efficient mechanism used for moving large amounts of data between I/O devices and main memory.

(ii) A process in the _____ state is loaded into main memory and available for execution.

(iii) _____ is a technique that allows the execution of processes which are not completely available in physical memory.

(iv) The problem of the processor spending the most of its time swapping pages and doing little productive work is called _____.

(v) A _____ is an operating system architecture where the entire operating system is working in kernel space and runs only in supervisor mode.

(vi) The process of putting data of various I/O jobs in a buffer, which is a special area in memory or hard disk which is accessible to I/O devices, is called _____.

(vii) A _____ is defined as an entity which represents the basic unit of work to be executed in a system.

(viii) _____ is a flow of execution through the process code, with its own program counter, system registers and stacks.

(ix) An address generated by the _____ is a logical address whereas address available on memory unit is a physical address.

(x) _____ is an operating system intended to serve applications that process data as it comes in, typically without buffer delays.

[02 x 10 Marks]