(15)
00103

The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Mechanical Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	: **DMX3304/ DMX3572/ MEX3272 Applied Electronics**
Academic Year	: 2019/20
Date	: 11th October 2020
Time	: 1330hrs – 1630hrs
Duration	: **3 hours**

WRITE YOUR REGISTRATION NUMBER CLEARLY WITHIN THE SPACE PROVIDED

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Eight (8)** questions in **Eight (8)** pages.
3. Answer any **Five (5)** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. This is a Closed Book Test (CBT).
6. Answers should be in clear hand writing.
7. Do not use Red color pen.

Question 01

a) Briefly explain the Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL).

[8 Marks]

b) Consider the Circuit diagram given below in Figure Q01.

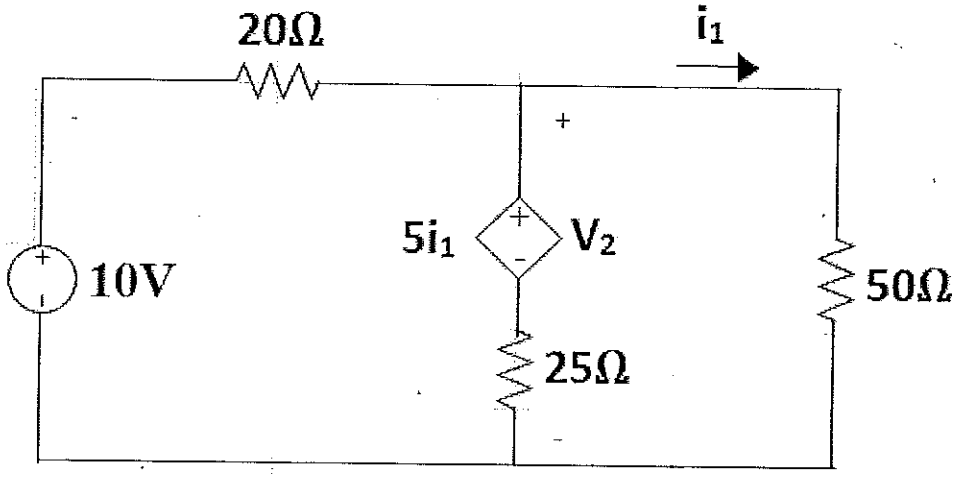

Figure Q01

i. Find the equations for the voltage V_2 and current i_1 in the circuit given in the Figure Q01, using nodal analysis.

[8 Marks]

ii. Solve the equations and find the values of V_2 and i_1.

[4 Marks]

Question 02

a) The circuit shown in Figure Q02(i), consists of two resistors R_1 and R_2 with resistances $R_1 = 6\ \Omega$ and $R_2 = 1.5\Omega$, one variable resistor R_{var}, one unknown resistor with value R_u, and a 9V battery connected.

When R_{var} is adjusted to 12Ω, there is zero current through the Ammeter. Find the unknown resistance R_u.

[10 Marks]

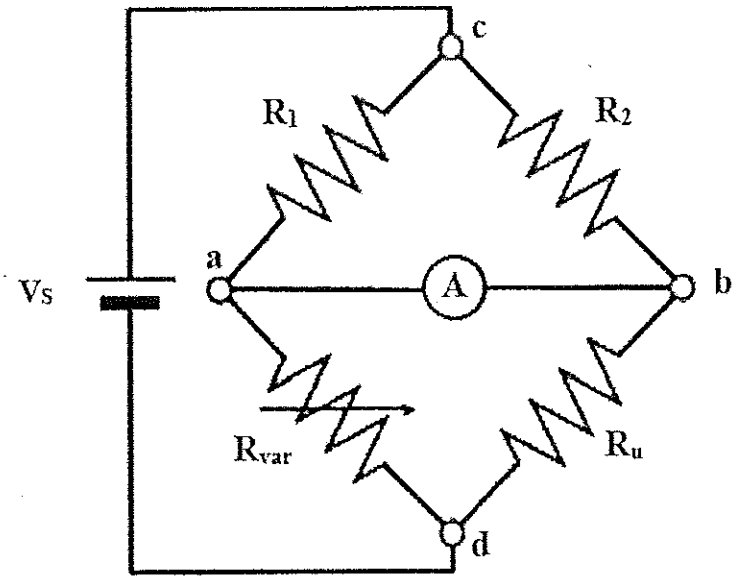

Figure Q02(i)

b) Determine I_D and V_{GS} for the JFET with voltage-divider bias shown in Figure Q02(ii). For this particular JFET, the internal parameters are such that V_D = 7V. (where, G-Gate, D- Drain, S-Source)

[10 Marks]

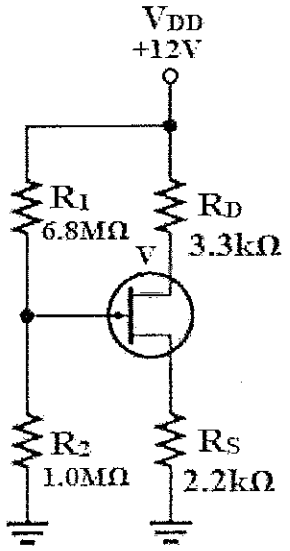

Figure Q02(ii)

Question 03

a) Draw the output characteristics for a BJT (Bipolar Junction Transistor) in CE (Common Emitter) Configuration. Label each region clearly.

[5 Marks]

b) In the circuit shown in the Figure Q03(i), the BJT has a current gain (β) of 50. If V_{EB} (Emitter – Base Voltage) is 600 mV, Find the V_{EC} (Emitter - Collector Voltage).

[7 Marks]

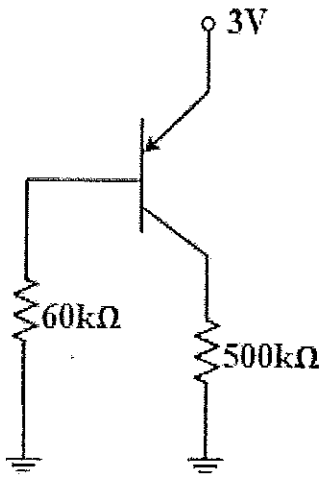

Figure Q03(i)

c) For a BJT circuit shown in Figure Q03(ii), assume that the 'β' of the transistor is very large and the V_{BE} (Base – Emitter Voltage) is 0.7 V. Determine the mode of operation of the BJT.

[8 Marks]

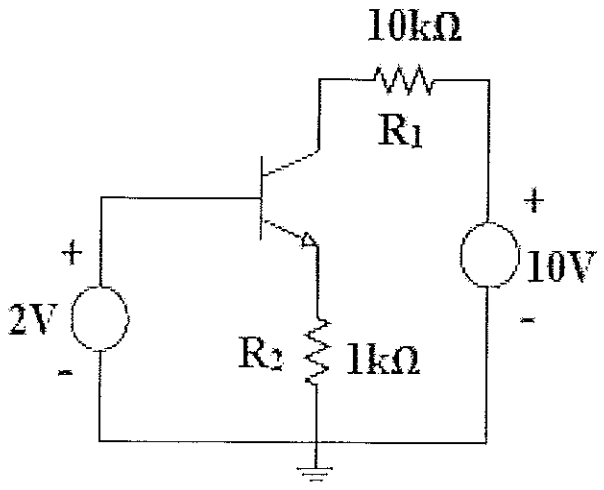

Figure Q03(ii)

Question 04

a) Briefly explain 4 characteristics of an ideal Op-amp.

[4 Marks]

b) For the ideal Op-amp shown in Figure Q04(i), Find the value of resistor R_f to obtain a gain of 5.

[6 Marks]

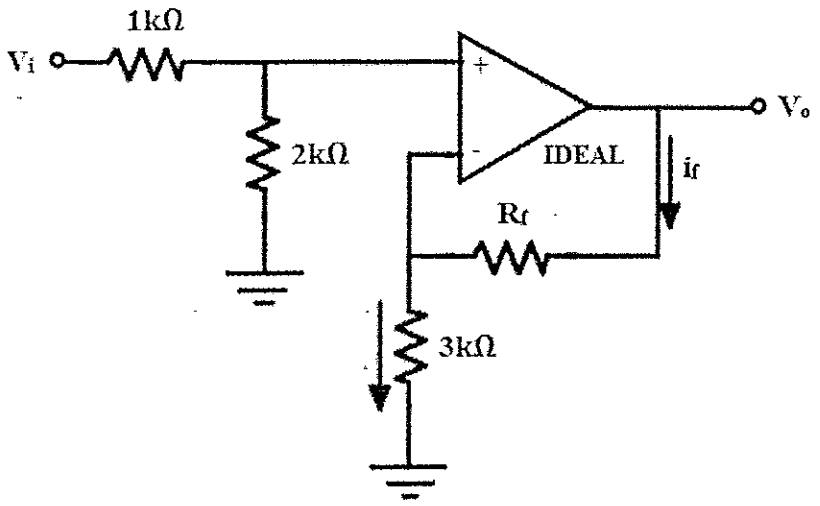

Figure Q04(i)

c) Evaluate the following amplifier circuit given in Figure Q04(ii), and Determine the value of resistor R_4 in order to obtain a voltage gain (V_o/V_i) of (-120).

[10 Marks]

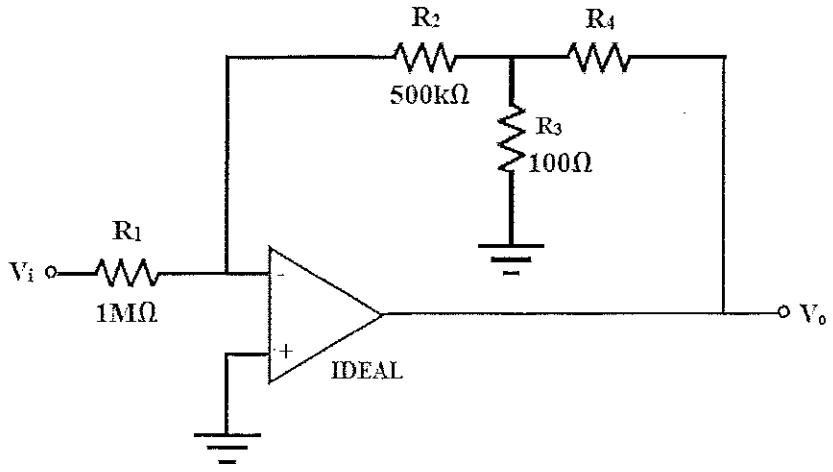

Figure Q04(ii)

Question 05

a) Draw circuit symbols of a diode and a Zener diode. Sketch the V/I characteristics of diode and Zener diode.

[4 Marks]

b) For the Zener diode regulator shown in Figure Q05(i), determine V_L, V_R and I_Z.

[5 Marks]

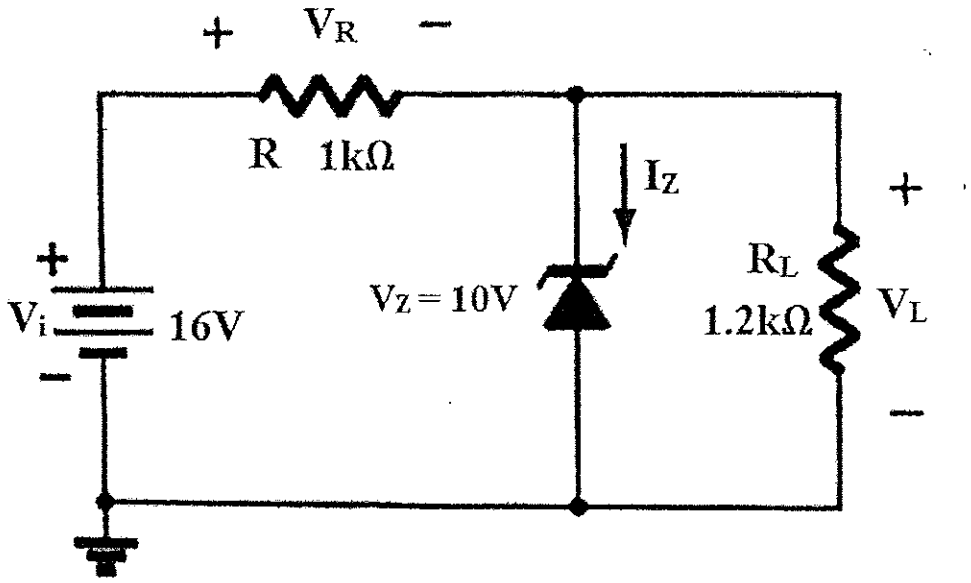

Figure Q05(i)

c) In the circuit shown in Figure Q05(ii), assume that the diodes D_1 and D_2 are Ideal. Find the average value of voltage V_{ab} (in volts) across terminals 'a' and 'b'.

[11 Marks]

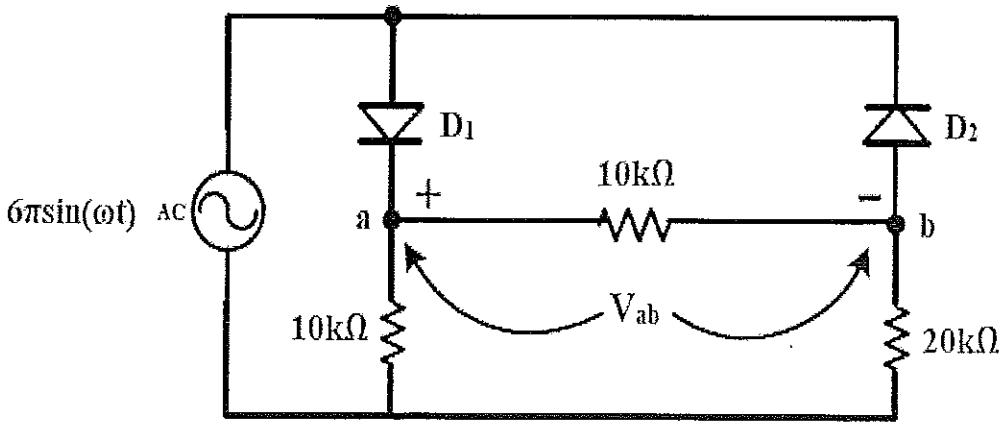

Figure Q05(ii)

Question 06

a) What are the main advantages of Hexadecimal numbering system?

[3 Marks]

b) Convert the number 35432_{16} (Hexadecimal) to Decimal number.

[4 Marks]

c) Determine the addition of the following numbers.

[4 Marks]

i. 00111001_2 to 00101001_2

ii. 10101.101_2 to 1101.011_2

d) Determine the multiplication of 1010_2 by 1011_2.

[4 Marks]

e) Determine the division of 11100110_2 by 110_2. State the quotient and remainder clearly.

[5 Marks]

Question 07

a) State the De' Morgan's theorem.

[4 Marks]

b) Prove the following Boolean Identities.

i. $A\,\overline{B}\,C + A\,B\,C + A\,B\,\overline{C} = A\,(B + C)$

[4 Marks]

ii. $A\,C + B\overline{C} = A\,B\,C + \overline{A}\,B\,\overline{C} + A\,B\,\overline{C} + A\,\overline{B}\,C$

[4 Marks]

c) The K-map for a Boolean function is shown in Figure Q07(i), Find number of essential prime implicants for this function.

[4 Marks]

CD \ AB	00	01	11	10
00	1	1	0	1
01	0	0	0	1
11	1	0	0	0
10	1	0	0	1

Figure Q07(i)

d) Use the K – Map technique and minimize the Boolean expression,

$$Y = \bar{A}\,\bar{B}\,\bar{C}\,D + \bar{A}\,B\,C\,\bar{D} + A\,\bar{B}\,\bar{C}\,D + A\,B\,\bar{C}\,\bar{D}$$

[4 Marks]

Question 08

a) Draw the symbols of the four Logic gates AND, OR, NAND and NOR for two inputs A and B.

[3 Marks]

b) Consider the Boolean function,

$$Z = A\,\overline{B}\,C$$

Find the minimum number of 2 input NAND gates required to implement the function above, assuming the inputs A, B, and C are available. (Hint: Draw the Logic gate diagram).

[4 Marks]

c) Consider the Boolean Expression,

$$X = AB + A\,B\,C + A\,\bar{B}\,\bar{C} + A\,\bar{C}$$

i. Draw the logic diagram for the expression.

[2 Marks]

ii. Minimize the expression.

[2 Marks]

iii. Draw the logic diagram for the reduced expression.

[2 Marks]

d) Prove the following expression by use of a truth table.

$$\bar{A}\,B\,\bar{C} + \bar{A}\,B\,C + \bar{A}\,\bar{B}\,C = \bar{A}\,B + \bar{A}\,C$$

[7 Marks]

END