THE OPEN UNIVERSITY OF SRI LANKA

Faculty of Engineering Technology
Department of Electrical & Computer Engineering
Bachelor of Technology Honours in Engineering – Level 6

FINAL EXAMINATION – (2014/2015)

ECX6151 – Digital Electronic Systems

Time Allowed: **3 hours**

Date: 18th September 2015 **Time: 0930 – 1230 hours**

INSTRUCTIONS TO CANDIDATES

1. This question paper contains one (1) question in **SECTION A** and four (4) questions in **SECTION B** on four (4) pages.
2. Answer **ALL PARTS** in **SECTION A**. [70 Marks]
3. Answer any **TWO (2)** questions from **SECTION B**. [30 Marks]
4. Refer the Annexure of the VHDL syntax given in page five (5) to write VHDL code.
5. Clearly state your assumptions if any

SECTION A: Answer ALL questions. [70 Marks]

Digital Electronic Filter Unit (DEFU)

The following scenario is about a Digital Electronic Filter Unit (DEFU) which is used for filtering unwanted noise in the optical encoder's outputs of a motor due to electromagnetic coupling and vibration in the operating environment. A pair of DEFUs, one for the channel A and the other one for the channel B, are required to filter out the noise on the incoming signals. Figure Q1 depicts the architecture of the DEFU.

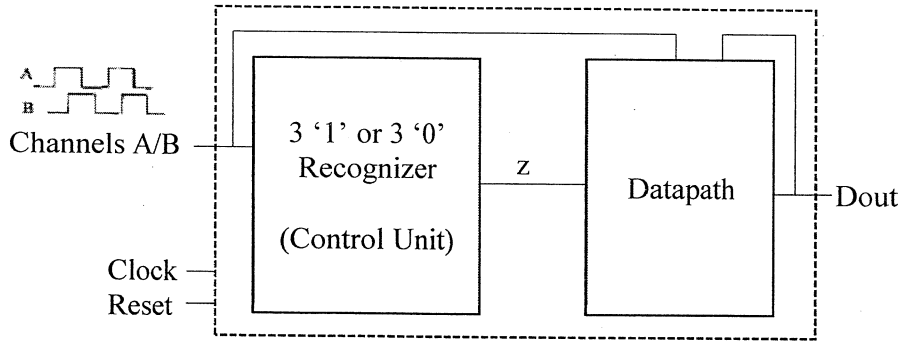

Figure Q1: Digital Electronic Filter Unit

The DEFU consists of a Control unit and a Datapath on each channel of the optical encoder. The Control unit is a recognizer that checks if the input from the optical encoder (Channel A/B)) has short duration pulses and then controls the input data to flow through the datapath, which consists of a 2: 1 multiplexer and a D flip-flop. If the input level has the same value (1 or 0) on at least three (3) consecutive clock cycles, then the input is not considered as a noise. In this case the output of the recognizer (z) is active high, which then allows the input data (Channels A/B) to flow through the datapath. The data value, thus becomes the new output of the DEFU. Otherwise the input is considered as a noise and the datapath output (Dout) of the DEFU remain the same.

Reference: Ming-Fa Tsai; Chien-Pang Chen, "Design of a quadrature decoder/counter interface IC for motor control using CPLD," in *IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the]* , vol.3, no., pp.1936-1941 vol.3, 5-8 Nov. 2002

Clearly state your assumptions (if any).

[Q1]

(i) Draw a circuit diagram for the Datapath of the DEFU. [05 Marks]

(ii) Draw a waveform of the DEFU. Clearly show the Channel A/B, z, Dout, and the Clock signals. [05 Marks]

(iii) Draw a state diagram for the Recognizer of the DEFU. [10 Marks]

(iv) Draw an ASM chart for the Recognizer of the DEFU. [10 Marks]

(v) Draw a state transition table for the Recognizer of the DEFU. [10 Marks]

(vi) Draw complete circuit diagram of the DEFU using D Flip-Flops and necessary digital logic gates. [20 Marks]

(vii) Write behavioral/structural VHDL code for the DEFU. [10 Marks]

SECTION B: Answer any TWO questions. [30 Marks]

[Q2] The internal connection diagram of a PLA is shown in the Figure Q2.

(i) Write the equations realized by the PLA. [06 Marks]

(ii) Specify the truth table for a ROM which would realize the same function. Clearly show the size of the ROM. [04 Marks]

(iii) Implement the ROM circuit of the truth table above (ii) using digital logic devices. [05 Marks]

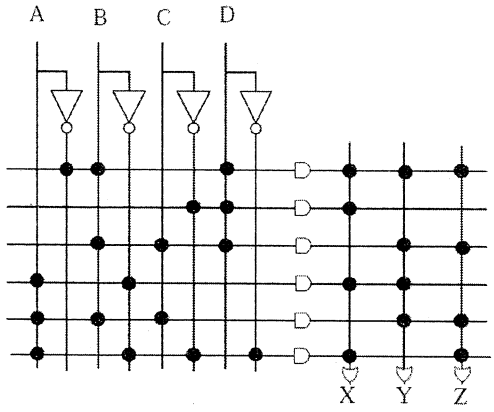

Figure Q2

[Q3]

(i) Derive the equations for 1 bit full adder. [03 Marks]

(ii) Implement the 1 bit full adder circuit using above (i). [04 Marks]

(iii) Write structural VHDL code of the 1 bit full adder circuit implemented in above (ii) [08 Marks]

[Q4] Consider the Boolean function $F(x, y, z) = \Pi(0, 3, 4, 5, 7)$.

(i) Draw the K-map for the function (F) and find a optimize expression for function (F). [08 Marks]

(ii) Implement the function (F) using 2 to 1 Multiplexers. [07 Marks]

[Q5] Consider the state table (Table Q5) given below.

(i) Reduce the state table (Table Q5) to a minimum number of states. [08 Marks]

(ii) Draw the reduced state table and state diagram. [07 Marks]

Table Q5

Present state	Next state $x=0$	Next state $x=1$	Output $x=0$	Output $x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

Annexure

Syntax of selected instructions of the VHDL

```
ARCHITECTURE architecture_name OF entity_name IS
  [declaration part]
BEGIN
  Concurrent statements part
END architecture_name
```

```
CASE expression IS
 WHEN value=> statements;
 WHEN value=> statements;
 WHEN OTHERS statements;
END CASE;
```

```
COMPONENT component_name
  PORT (port1_name : port1_type;
        port2_name : port2_type;
        …);
END COMPONENT [component_name];
```

```
ENTITY entity_name IS
  PORT (port1 : port1_type;
        port2 : port2_type;
        …);
END entity_name;
```

```
IF condition THEN
  Sequence of statements
  {ELSIF condition THEN
     Sequence of statements}
[ELSE
  Sequence of statements]
END IF;
```

```
LIBRARY library_name;
```

```
Instance_label: component_name PORT MAP (first_port, second_port,
                                         third_port, …);
Instance_label: component_name PORT MAP (formal1=> actual1,
                                         formal1=> actual1,
                                         formal1=> actual1, …);
```

```
[process_label:] PROCESS (signal1, signal2, …)
                   [declaration part]
                 BEGIN
                   Sequential statements part
                 END PROCESS;
```

```
SIGNAL signal_name : signal_type;
```

```
TYPE type_name;
```

```
USE library_name.type_expression.inclussion;
```

```
WAIT FOR time_expression;
WAIT ON signal1, signal2, …;
WAIT UNTIL condition;
```

```
WHILE condition LOOP
  Sequential statements
END LOOP;
```