The Open University of Sri Lanka
Faculty of Natural Sciences
B.Sc/ B. Ed Degree Programme

Department	: Physics
Level	: 05
Name of the Examination	: Final Examination
Course Code and Title	:**PHU5318 – Electronics for Biology Students**
Academic Year	: 2020/2021
Date	: 2021-12-15
Time	: 9.30 am – 11.30 am
Duration	: 02 hours

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of 06 questions in 06 pages.
3. Answer any **04** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. Draw fully labelled diagrams where necessary
5. Relevant log tables are provided where necessary.
6. Having any unauthorized documents/ mobile phones in your possession is a punishable offense.
7. Use blue or black ink to answer the questions.
8. Circle the number of the questions you answered in the front cover of your answer script.
9. Clearly state your index number in your answer script

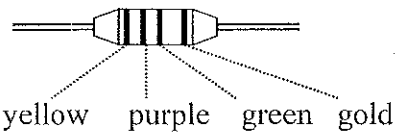
The Open University of Sri Lanka
B.Sc./B.Ed. Degree Programme - Level-03
Final Examination - 2020/2021
PHU5318 - Electronics for Biology Students
Duration : Two (2) hours

Date : 15th December 2021 **Time: 9.30 a.m.- 11.30 a.m.**

Answer Four(4) questions only

(1) (i) Find the resistance of the followings

(a) Resistor

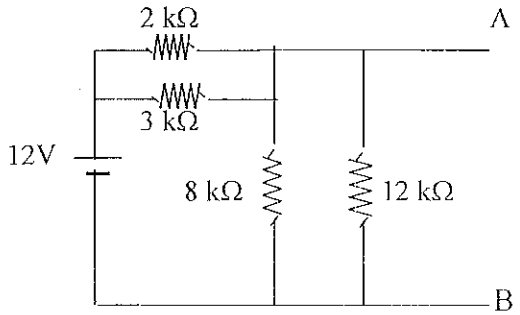


Yellow - 4
Green - 5
Purple -7
Gold - 5%

(b). Charged capacitor connected with a 1k resistor in parallel.
(c). Reversed biased diode.

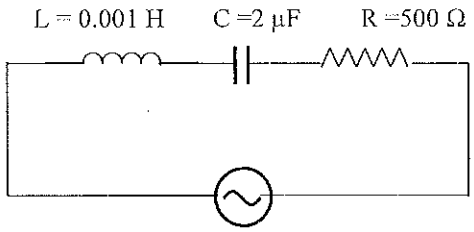
(ii) An LED is operated at 2.2V/ 40 mA. If you are given a 9 V battery , how do you light up this LED ?

(iii) Write down the Thevenin's equivalent circuit theorem. Draw the Thevenin's equivalent circuit for the following resistor and voltage network.



(iv) When two resistors are connected in parallel, the resultant resistance decreases. But when two capacitors are connected in parallel, the resultant capacitance increases. How do you explain these differences?

(2) The following figure shows a circuit consisted of ac voltage source ; V = 300 cos(650 t) mV , an inductor (0.001H), a capacitor (2 μF) and a resistor (500 Ω).



V = 300 cos(650 t) mV

(i) Draw the phasor diagram for the voltage across each component.

(ii) Obtain a general expression for the total impedance for the circuit with L, C, R and angular frequency; ω

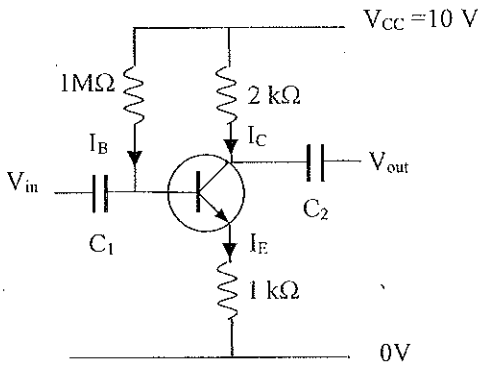
(iii) Hence calculate the total impedance of the circuit.

(iv) Calculate the peak current through the circuit .

(v) What is the phase difference between the current through the circuit and the voltage across the resistor ?

(vi) Explain how this circuit is converted to a resistive (only resistance effect) circuit balancing the values of other two components (C and L)

(3) The following single stage transistor amplifier is constructed with a NPN bipolar junction Si transistor in which the Base-emitter voltage drop (V_{BE}) is 0.7 V and the current gain (β) is 100.



(i) Obtain an equation with I_B and I_E, considering the voltage drops across the resistors 1 MΩ, 1 kΩ and Base-Emitter.

(ii) Write down the current I_C in terms of I_B hence I_E in terms of I_B.

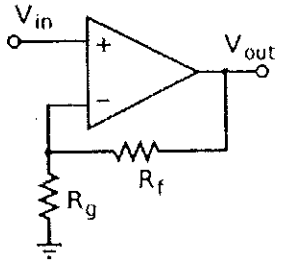
(iii) Now using the equation obtained in (i) and (ii) find I_B, I_C and I_E.

(iv) What is the voltage across the collector and emitter (V_{CE})

(v) A bypass capacitor; 1 μF is used across R_E (=1 kΩ) to avoid noise amplification. Calculate the frequency of the noise signal at which the impedance of the capacitor is 1/10 of R_E. Explain that the performance of the amplification is better when the noise frequencies are higher than the above frequency.

(vi) A low cost transistor radio which is operated with dc power pack without any voltage regulation, works properly at lower volume. But when the volume increases, it is observed a sound distortion. What could be the reason for this fault?

(4)The following figure shows the circuit diagram of a non-inverting amplifier.

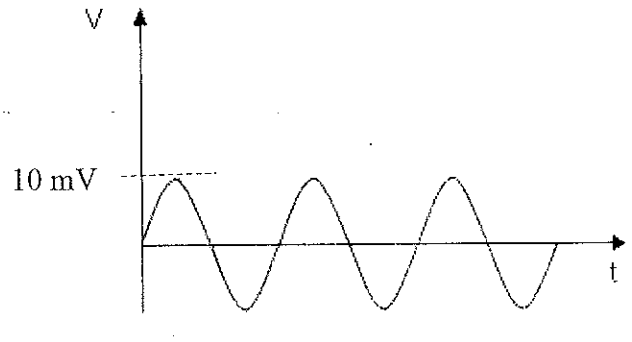


(i) Obtain the expression for the output voltage gain

$$\frac{V_{out}}{V_{in}} = (1 + \frac{R_f}{R_g})$$

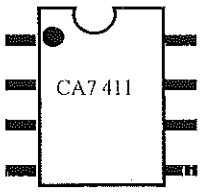
assuming the golden rules for operational amplifiers .

(ii) (a) A student wants to amplify the following voltage signal with the voltage gain of 101 . Suggest suitable values for R_f, , R_g and for voltages (± V) of a dual power supply to activate the circuit . Justifications for your suggestions should be given .



(b) The student used a collection of dry cells to construct his dual power supply . After using the above supply he observed a distortion at output voltage signal . Give a reason for this defect.

(c) The following information are for a general purpose operational amplifier ; CA741



Pin No: 1 Off set null
Pin No: 2 Inverting input
Pin No: 3 Non inverting input
Pin No: 4 Negative power supply
Pin No: 5 Off set null
Pin No: 6 Output
Pin No: 7 Positive power supply
Pin No: 8 No connection

Redraw the above IC on your answer script and complete the above circuit with symbols of other components.

(iii) " A non inverting amplifier circuit is more suitable for amplifying the voltage signal produced by the electrodes of a pH meter compared to the inverting amplifier circuit " Comment on this statement.

(5).(i) Write down a truth table for the logic circuit that has three inputs, A, B, and C, and whose output will be HIGH only when a majority of the inputs are HIGH.

(ii) Obtain the Boolean expression for the output of the circuit.

(iii) Simplify the above expression into two input AND gates and three input OR gate . (Hint: $P + \bar{P} = 1$ where P is any logic input)

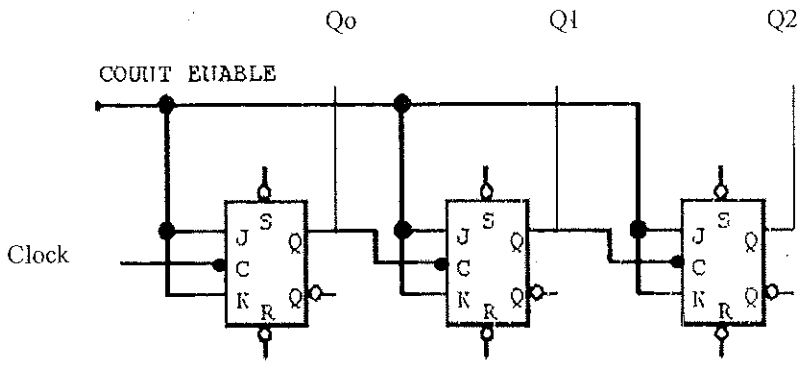
(iv) Implement a circuit for the final expression .

(v) A one type of jewellery locket used in a Bank is opened identifying the faces of any two persons out of three authorized officers. Another type of jewellery locket is opened identifying the faces of two or more persons out of three authorized officers in the Bank. Which security system is more secured? Justify your answer.

(6) (i)The output of a sequential logic circuit is decided based on the existing output state and the input combination . But that of a combinational logic circuit is decided based only on the combination of inputs' states. Explain these statements giving simple examples for each type o these logic circuits.

(ii) Write down the truth table of a J-K Flip flop.

The following diagram shows a three bit ripple counter



(iii) If each J-K flip flop activates at the falling edge of the clock pulse, draw the waveform at each binary output ; Qo, Q1 and Q2 for ten (10) clock pulses.

(iv) How do you modify this circuit to reset the output after 6 clock pulses?

(v) What is given by the combination of $\bar{Q}$ outputs ; Qo Q1, Q2 ?

(vi) In a digital clock which parameter is mostly responsible for the accuracy of the time ?

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