The Open University of Sri Lanka
Faculty of Natural Sciences
B.Sc/ B. Ed Degree Programme

Department	**: Computer Science**
Level	**: 05**
Name of the Examination	**: Final Examination (1st Semester)**
Course Title and - Code	**: CSU5306 – Digital Electronics**
Academic Year	**: 2020/2021**
Date	**: 28/12/2021**
Time	**: 1.30pm – 3.30pm**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **06** questions in **05** pages.
3. Answer any **04** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. Draw fully labelled diagrams where necessary
6. Involvement in any activity that is considered as an exam offense will lead to punishment
7. Use blue or black ink to answer the questions.
8. Clearly state your index number in your answer script

THE OPEN UNIVERSITY OF SRI LANKA

DEPARTMENT COMPUTER SCIENCE

B. SC. DEGREE PROGRAMME 2020/2021

FINAL EXAMINATION

CSU5306: DIGITAL ELECTRONICS

DURATION: TWO HOURS (2 HOURS)

Date: 28.12.2021 **Time: 1.30 pm – 3.30 pm**

Answer **FOUR** (04) Questions **ONLY.** All questions carry equal marks.

Q1.

i. Convert the following binary (base 2) numbers into decimal. Clearly show the steps.

   a. 1101

   b. 10011

ii. Convert the following decimal numbers into binary. Clearly show the steps.

   a. 69

   b. 278

iii. Convert the binary values derived in (ii) into Hexadecimal and Octal. Clearly show the steps.

iv. Prove the following Boolean Algebra Rules. Clearly show the steps.

   a. Associative Law

   b. De Morgan's Theorem

v. Agricultural plant uses three tanks to store grain that is required to dispatch to farmers. Each tank has a sensor that detects when the grain level drops to 25% of full. The sensors produce a 5V level when the tanks are more than one-quarter full. When the volume of grain in a tank drops to one quarter full, the sensor puts out a 0V level. It is required that a Red Light-Emitting Diode (LED) on an indicator panel lights when two tanks are more than one - quarter full. Show how a NAND gate can be used to implement the function.

Q2.

i. Simplify the following Truth Table using Minterm Canonical form.

A	B	C	Q
0	0	0	0
0	1	0	1
0	0	1	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

ii. Draw the simplified logic circuit.

iii. Redraw the circuit in (ii) using any universal logic gate.

iv. Draw the Timing Diagram for the output Q (in i) according to the inputs.

v. Assuming a propagation delay through each gate of 10 nanoseconds (ns), determine if the desired output waveform Q in the truth table (in i) (a pulse with a minimum tw= 25ns positioned) will be generated properly with the given inputs. (Clearly state the steps).

Q3.

i. Derive the Truth Table for a four (4) bit Parallel Binary Adder

ii. Draw the Adder circuit (in i) with the help of the schematic diagram for the one-bit adder circuit.

iii. Draw the logic diagram of the Binary Decoder for 1011(in base 2)

iv. Draw the block diagram of the 2-1 multiplexer.

v. Using the 2-1 multiplexer, develop a 16-1 Multiplexer.

Q4.

i. Describe the difference between Combinational logic and Sequential logic with the help of diagrams.

ii. Explain the function of the SR flipflop. Use Logic circuit, Truth Table and Timing Diagram as needed.

iii. Draw the IC circuit for the Master Slave flip flop using JK flip flops (74HC76)

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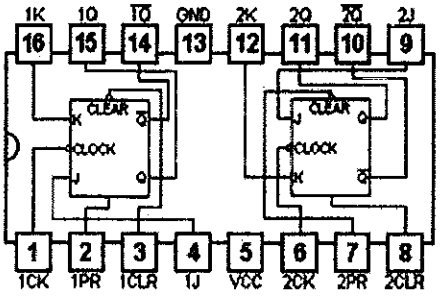

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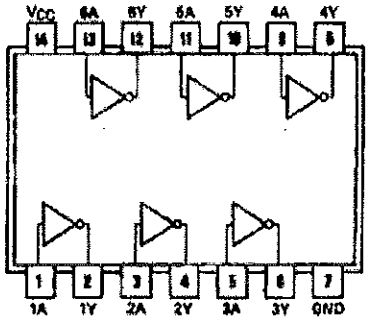


iv. Derive the asynchronous sequential circuit for the circuit described by the following State Table. Clearly show the steps.

Present State		Next State			
		X = 0		X = 1	
0	0	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	1	1	1	1	0

v. Discuss the stability of the above circuit (in iv).

Q5.

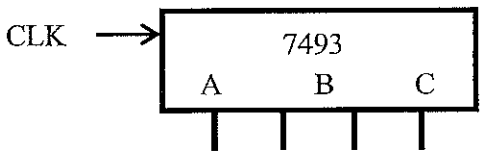
i. Registers are used for special purposes in the computer. Name 5 of them and state their use.

ii. Describe how to convert 4-bit serial data to parallel data using block diagrams of register circuits.

iii. Edge triggered JK flip flops can be used for counters. Explain the counting function of an array of 4-bit JK flip flops using a timing diagram.

iv. Draw the counter circuit to count to 9 using a synchronous counter circuit block diagram.

v. Explain how a divide by n counter can be used as a frequency divider. Use TTL 7493 IC as an example to describe the function.



Q6.

i. Briefly explain the components of the CPU that are used in the Fetch and Execute cycle.

ii. Draw the one-bit memory cell using D- flip flop.

iii. Explain the Data Write and Data Read functions using the diagram in (ii).

iv. Derive a 16-bit RAM using one-bit memory cell in (ii).

v. Implement the logic circuit of the PLA using following Boolean functions.

$F1 = AB' + AC + A'BC$

$F2 = (AC + BC)'$

-End of Examination Paper –