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087

The Open University of Sri Lanka
Faculty of Natural Sciences
B.Sc./ B. Ed Degree Programme

Department	**: Computer Science**
Level	**: 05**
Name of the Examination	**: Final Examination (2nd Semester)**
Course Title and - Code	**: CSU5310– Computer Architecture**
Academic Year	**: 2020/2021**
Date	**: 04/04/2022**
Time	**: 1.30 pm – 3.30 pm**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **06** questions in **04** pages.
3. Answer any **04** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. Draw fully labelled diagrams where necessary
6. Involvement in any activity that is considered as an exam offense will lead to punishment
7. Use blue or black ink to answer the questions.
8. Clearly state your index number in your answer script

THE OPEN UNIVERSITY OF SRI LANKA

DEPARTMENT COMPUTER SCIENCE

B. SC. DEGREE PROGRAMME 2020/2021

FINAL EXAMINATION

CSU5310: COMPUTER ARCHITECTURE

DURATION: TWO HOURS (2 HOURS)

Date: 04.04.2022 **Time: 1.30 pm – 3.30 pm**

Answer **FOUR** (04) Questions **ONLY.** All questions carry equal marks.

Q1.

i. Group following attributes into two groups: Architectural Attributes and Organizational Attributes.

Instruction Set, Memory Technology, Control Signals, I/O mechanism, Interfaces between the computer and peripherals, Number of bits used to represent data, Technology for addressing memory, Hardware details transparent to programmer

ii. What are the uses of major structural components in the CPU?

iii. What is implied by the "top level view of structure and function of the computer"?

iv. Discuss this statement "Changes in technology not only influence organization but also result in the introduction of more powerful and more complex architecture".

Q2.

i. What are the states of an instruction cycle?

ii. Compare the two modes of programming: Hardware Approach, Software Approach. (Use a diagram if necessary)

iii. Draw a diagram to describe Instruction Cycle with interrupts.

iv. Discuss an example scenario where interrupts are used to improve the processing efficiency.

Q3.

i. What are the transactions that must be supported by the interconnection structure?

ii. Briefly describe the four methods of accessing units of data in memory.

iii. Describe the function of Cache memory using a diagram.

iv. "The characteristic we see when going down a typical memory hierarchy is that smaller, more expensive, faster memories are supplemented by larger, cheaper, slower memories." Comment on this statement.

Q4.

i. What are the properties common to all semiconductor memory cells?

ii. Describe the operation of the memory cell with reference to three functional terminals capable of carrying an electrical signal.

iii. Compare DRAM and SRAM.

iv. Discuss the disadvantages of wiring data into the ROM chip as part of the fabrication process.

Q5.

i. Draw a diagram to describe the IO Module.

ii. Write the steps in involve in the control of the transfer of data from an external device to the processor.

iii. Two essential tasks of an I/O module are data buffering and error detection. Briefly describe them.

iv. Compare Batch multiprogramming and Time-Sharing Operating system features.

Q6.

i. The set of machine instructions must be sufficient to express any of the instructions from a high-level language. What are the categories of instructions used?

ii. Draw a diagram to present simple instruction format.

iii. Briefly define following terms related to addressing.

   a. immediate addressing.
   b. direct addressing.
   c. indirect addressing.
   d. register addressing.
   e. register indirect addressing.
   f. displacement addressing.
   g. relative addressing.

iv. Discuss about the most fundamental issues relating to the design of instruction sets?

-End of Examination Paper –