THE OPEN UNIVERSITY OF SRI LANKA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
BATCHELOR OF TECHNOLOGY

FINAL EXAMINATION - 2014/2015

ECX6330 –ELECTRONIC SYSTEMS **(Closed Book)**

ANSWER ANY FIVE QUESTIONS.

Date 16.09.2015 ***Time: 9:30-12:30 hrs.***

Q1. Consider the circuit in the Figure-Q1 with Si transistors.

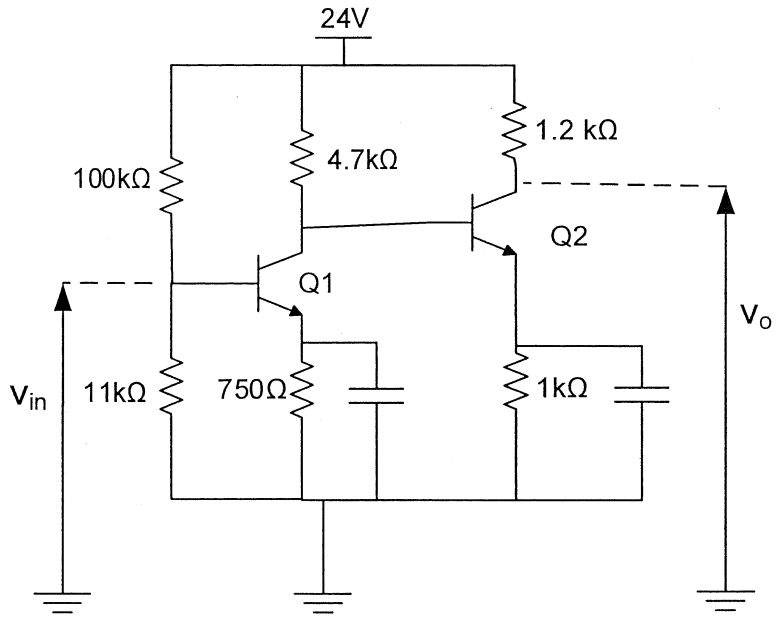

Figure-Q1

Q1: $\beta = h_{fe} = 100, h_{ie} = 1k\Omega$

Q2: $\beta = h_{fe} = 60, h_{ie} = 1.4k\Omega$

You may assume that the effect from h_{oe} and h_{re} are negligible.

(a) Find the quiescent values of V_{CE1}, I_{C2}, V_{C2} and V_{CE2}. **(8 Marks)**

(b) Draw the low frequency equivalent circuit. **(6 Marks)**

(c) Find the mid band voltage gain $\frac{V_o}{V_{in}}$. **(6 Marks)**

Q2. The transistor in Figure-Q2 has the a low frequency β of 120, $r_e = 20\Omega$ and $r_o = 100k\ \Omega$. The inter-electrode capacitances are $C_{be} = 40pF$, $C_{bc} = 1.5pF$ and $C_{ce} = 5pF$. There is a wiring capacitance equal to $4pF$ across the input and $8pF$ across the output.

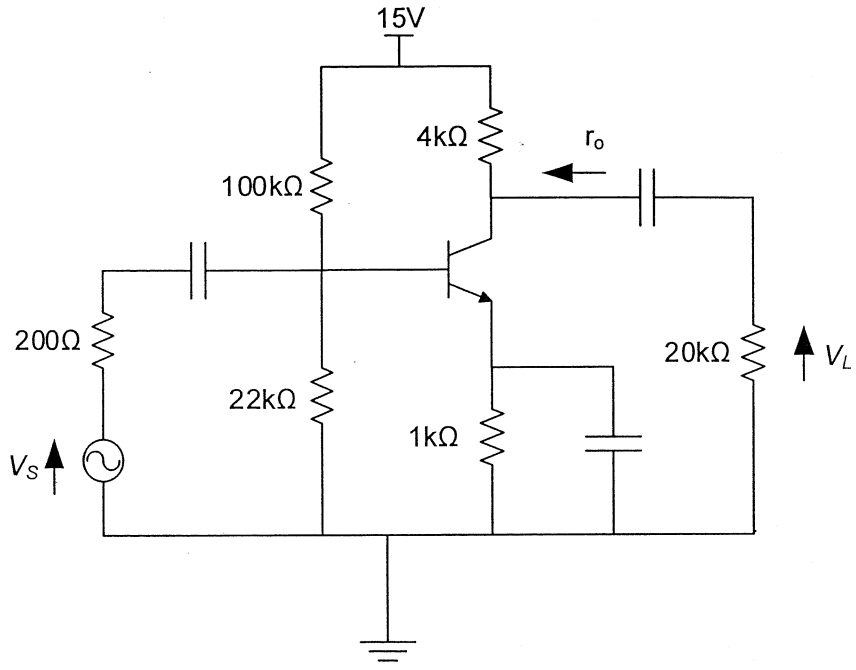

Figure-Q2

(a) Draw the high frequency equivalent circuit for this amplifier circuit. **(6 Marks)**
(b) Calculate the input and output impedances. **(8 Marks)**
(c) Hence, find the approximate upper cutoff frequency of this amplifier. **(6 Marks)**

Q3.

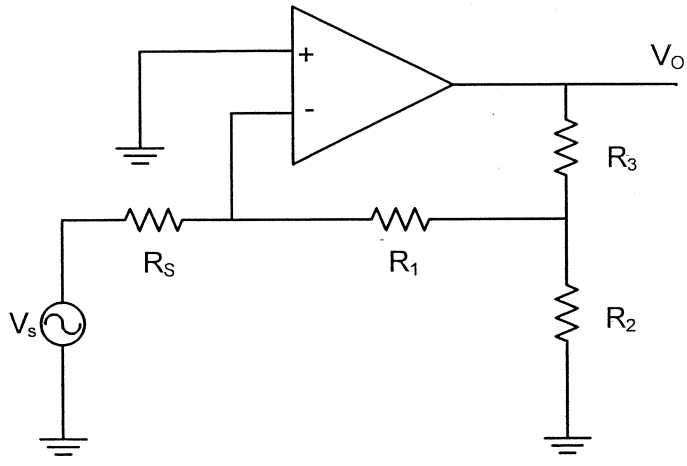

Figure –Q3

Consider the feed-back arrangement in the above Figure-Q3 circuit diagram. Let the open loop gain of the op-amp is 10,000 and the source input resistance is $100k\Omega$.

$R_1 = R_3 = R_S = 1k\Omega,\ R_2 = 100k\Omega.$

a) Identify the type of feed-back used. **(2 Marks)**
b) Calculate the feedback factor, considering the effect of the input resistance. **(8 Marks)**
c) Let the amplifier is connected with a load $R_L = 1k\Omega$. Calculate the total closed-loop gain considering the effects of load and input resistances. **(10Marks)**

Q4.

(a) Draw the transfer characteristic curves for ideal and non-ideal comparators and compare them. **(4Marks)**

(b) The one shot circuit shown in Figure-Q4 is having $v_O = L+$, $v_A = 0$ and $v_B = -V_{Ref}$ in the stable state. The circuit is triggered by applying a positive input pulse greater than V_{Ref}. Assume that $R_1C_1 \ll RC$.

i. Sketch the waveforms of v_A and v_O along with the trigger pulse. **(4Marks)**
ii. What is the width of the pulse (T) generated at the output? **(4Marks)**
iii. Explain how T can be controlled. **(3Marks)**

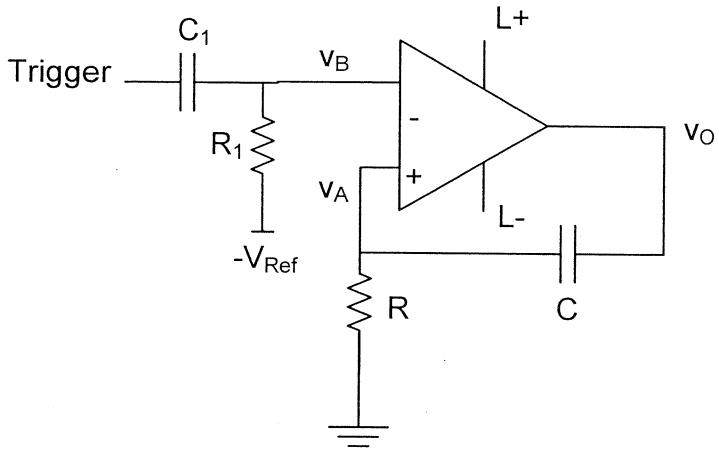

Figure-Q4

(c) Draw the circuit diagram of a free running square wave generator using a Schmitt trigger circuit. **(5Marks)**

Q5. (a) Starting from the first principles derive the Barkhausen criterion for the oscillations to occur. **(4 Marks)**

(b) The circuit diagram of a Wien-Bridge oscillator is shown in Figure-Q5. Calculate,

i. The range of R variation required to obtain oscillations in the range of $10kHz - 50kHz$. **(10 Marks)**

ii. R_f value required for oscillations to occur at $10kHz$. **(6 Marks)**

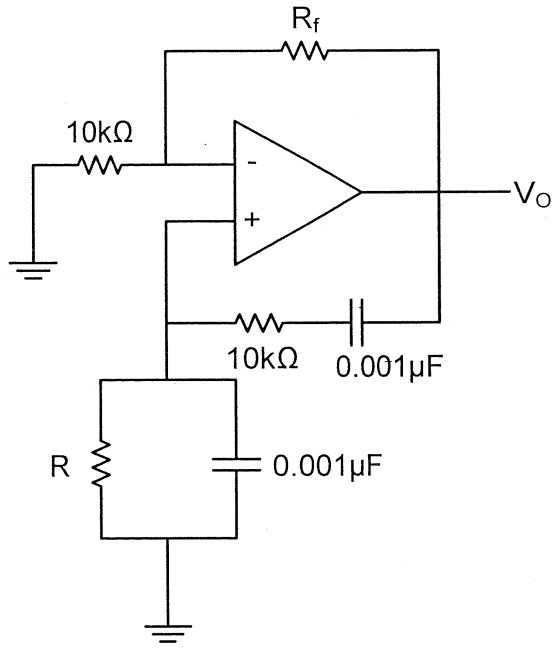

Figure –Q5

Q6.

(a) Starting from the diode characteristic equation $I_D = I_S\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$ derive an expression for the intrinsic resistance, r_e of the diode junction. **(4 Marks)**

(b) Figure-Q6 (b) shows a diode-based log amplifier. Show that $V_o \propto \ln(V_{in})$. **(8 Marks)**

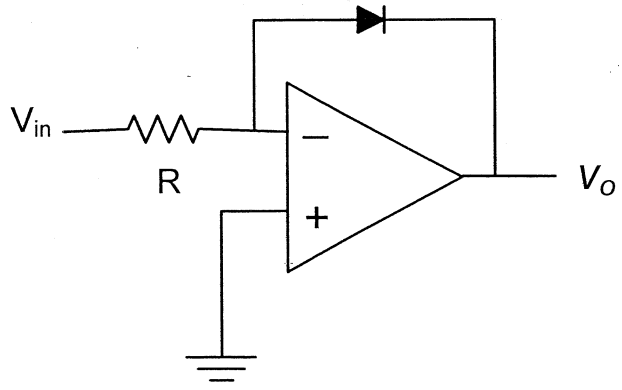

Figure-Q6 (b)

(c) Explain the operation of the precision rectifier arrangement shown in Fig-Q6 (c). **(8 Marks)**

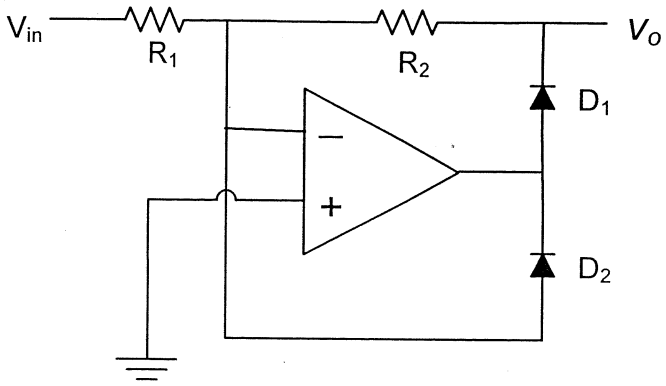

Figure-Q6 (c)

Q7.

(a) Compare successive approximation type, flash and counter type ADCs in terms of their conversion speed, resolution and cost. **(6Marks)**

(b) Using suitable diagrams, explain the operation of a successive approximation type ADC. **(5Marks)**

(c) A certain successive approximation type 8 bit ADC can handle input voltages in the range $0 - 8V$. Find,

i. The resolution of the ADC. **(3Marks)**

ii. The conversion speed of the ADC for a $1MHz$ clock. **(3Marks)**

(d) Sketch the plot of DAC output voltage vs time for a conversion of $3.2V$. **(3Marks)**

Q8.

(a) Give the main difference between the following.

i. ROM and EEPROM
ii. PLA and PAL
iii. Static RAM and Dynamic RAM **(2 x 3 Marks)**

(b) Carry look ahead adder is a concept used in modern microprocessor ALUs to generate all carry bits required in adding two multi bit numbers using a combinational circuit. This eliminates the need for long waiting in order to receive the rippled carry bits. Let $A = a_4a_3a_2a_1$ and $B = b_4b_3b_2b_1$ are two 4 bit numbers for addition. Consider the addition of a single bit position with a full adder.

i. Show that the Boolean expression for the carry at the n-th bit ($n = \{1,2,3,4\}$) can be expressed in the form $C_n = G_n + C_{n-1}P_n$ where G_n and P_n are Boolean functions of $a_n$and b_n.
[You should clearly show the steps including the truth table and minimization]
(4Marks)

ii. Hence show that C_n can be expressed interms of c_0, a_n and b_n only ($n = \{1,2,3,4\}$). **(4Marks)**

iii. Implement the complete carry generation combinational logic circuit with a PLA. **(6Marks)**