The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Mechanical Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: DMX5570 / MEX5270**
Academic Year	: 2019/2020
Date	: 13th October 2020
Time	: 0930-1230 hrs
Duration	**: 3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Seven (7)** questions in **Six (6)** pages.
3. Answer any **Five (5)** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. This is a Closed Book Test **(CBT)**.
6. The symbols used in this paper have their usual meanings.
7. Clearly state any assumptions that you may make.
8. Answers should be in clear handwriting.
9. Do not use red colour pen.

Question 1

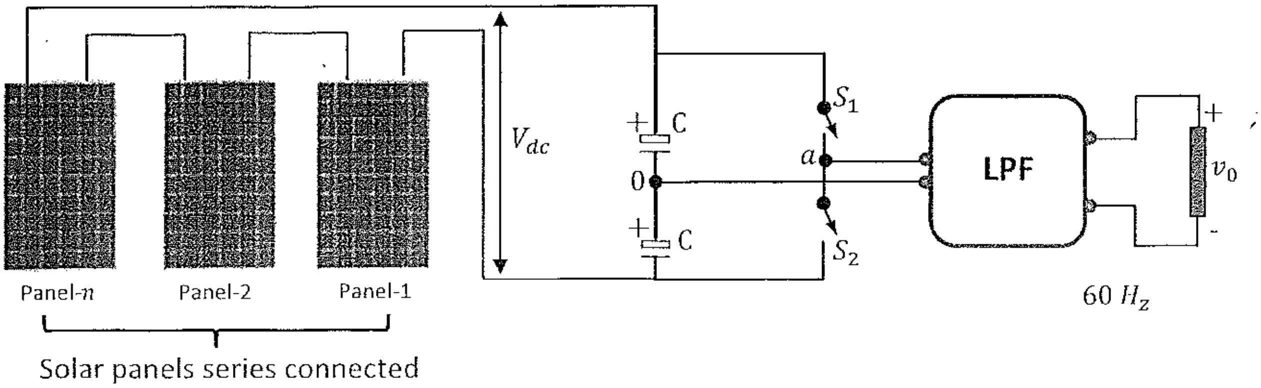

Figure Q1 (a): Grid-tie string inverter system

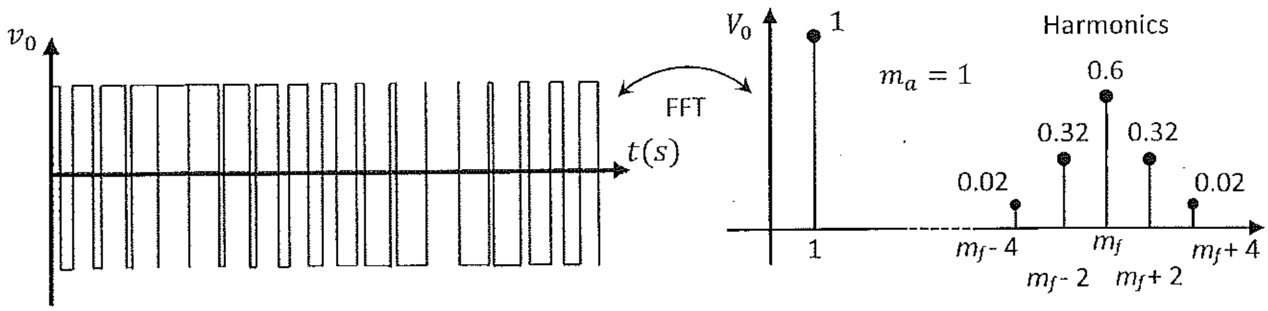

Figure Q1 (b): Waveforms in time and frequency domains for the output voltage of a PWM, DC to AC inverter

As shown in figure Q1 (a), photovoltaic solar system architecture with the string inverter employs a central conversion unit. The amplitude modulation index and frequency modulation index are defined respectively by $m_a = V_0^*/V_t$ and $m_f = f_t/f_0$: where V_0^* and V_t are the amplitudes of the reference voltage and carrier signal, while f_0 and f_t are the frequencies of the reference voltage and carrier signal, respectively. Figure Q1 (b) shows the output voltage v_0 in the time domain and in the frequency, domain obtained through Fast-Fourier-Transformation (FFT). If the voltage shown in figure Q1 (b) is from a PWM DC to AC central converter with frequency (f_0) equal to 60 Hz and $m_a = 1$, determine the following:

a) what is the frequency of the harmonic components with magnitude 0.32?

b) what is the RMS value for all the harmonics presented in figure Q1 (b) if $V_{dc} = 500\ V$?

Note: The switching frequency of this converter is 1260 kHz.

(20 Marks)

Question 2

a) List and describe how Snubber circuits can be used to significantly reduce switching stresses on power semiconductor devices.

b) Sketch the voltage and current waveform for a turn-on snubber circuit network and for a turn-off snubber circuit network for the period $0 \leq t \leq t_2$.

c) A power semiconductor switch experiences a linear fall in electric current from 50 A to 0 A in 1.5 μs at turn-off. At turn-on the power semiconductor switch experiences a linear fall in voltage from its off-state value of 200 V to 0 V in 1.2 μs.

   i) Determine the value of the capacitor in the snubber network if the voltage rise-time is delayed to 0.5 μs, 1.0 μs and 1.5 μs.

   ii) Determine the losses at each condition mentioned in (part c (i)) and suggest a suitable value of the snubber resistance. Assume that the $t_{on(min)} = 10\ \mu s$.

d) Determine the value of the inductor in the snubber network if the current rise-time is delayed to 0.4 μs, 0.8 μs and 1.2 μs.

   iii) Determine a suitable value for the snubber resistance. Assume that the $t_{off(min)} = 5\ \mu s$.

(20 Marks)

Question 3

a) Describe the characteristics of a Four-Layer Diode by taking into consideration its *i-v* characteristic curve.

b) State all the essential points on the *i-v* characteristic curve.

c) i) Distinguish between DIAC and TRIAC in reference to power electronics.

ii) How these components that mentioned in (part c (i)) differ from a SCR.

d) Draw the *i-v* characteristic curve for a DIAC and TRIAC.

e) As shown in figure Q3 (a) and figure Q3 (b) by taking into consideration the voltage and current of the power switches employed in the circuits (circuit 1 and circuit 2):

i) draw the voltage vs time graphs and the current vs time graphs for each power switch.

ii) define the static characteristics (*i-v* characteristic curve) of the power switches employed in the circuits

Notice that the abscissa of the waveforms in figure Q3 (a) and figure 3Q (b) is given in seconds instead of *rad*.

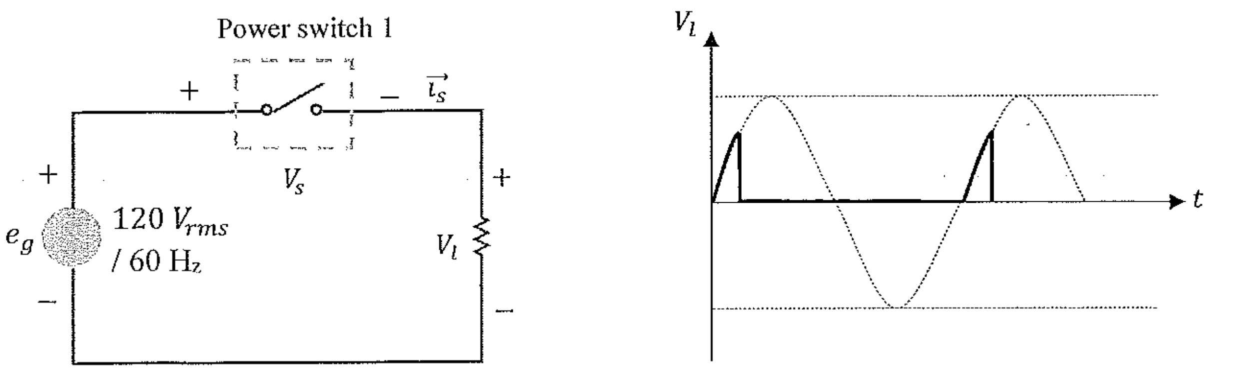

Figure Q3 (a): Circuit 1 and its load voltage

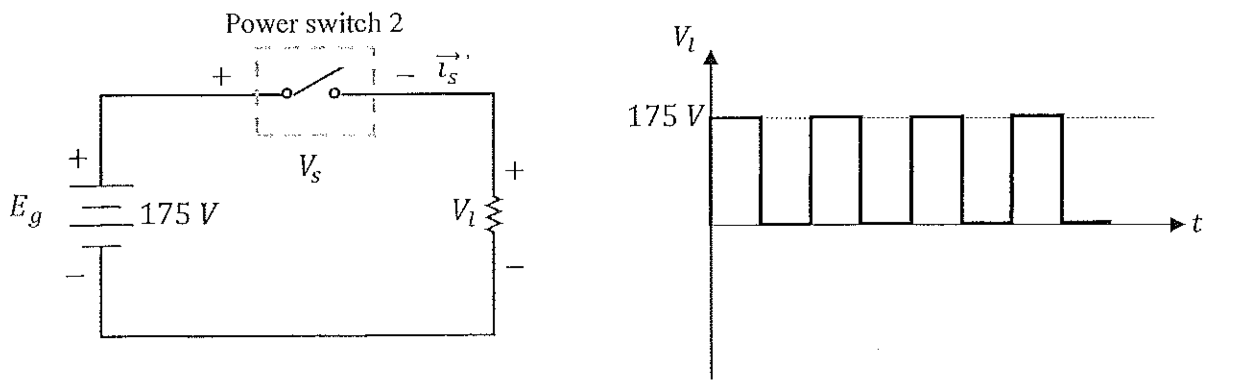

Figure Q3 (b): Circuit 2 and its load voltage

(20 Marks)

Question 4

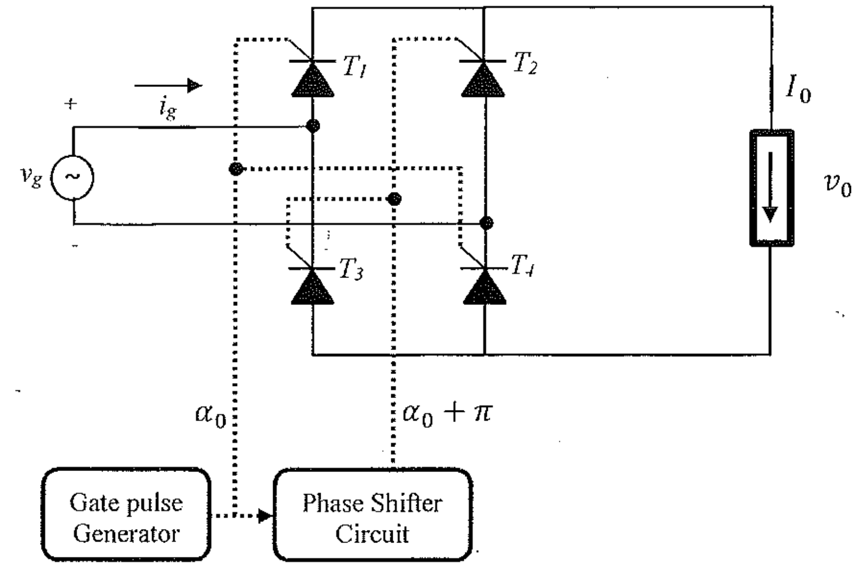

Figure Q4: Single-phase thyristor rectifier supplying a strong-inductive load

a) As shown in figure Q4, the single-phase rectifier circuit needs to implement using thyristors and where the mentioned load has strong inductive properties which are represented by a current source.

i) Plot the load voltage and the grid current waveforms.

ii) Determine the average load voltage as a function of the gate pulse angle (α - firing angle) and E_g.

b) Now if an inductor $L_g$in series with the voltage source v_g:

i) sketch the load voltage and the load current waveforms

ii) sketch the load voltage and the gate signals waveforms

iii) derive an expression in terms of circuit parameters such as ω_g, L_g, e_g and I_0 for the interval of time (Δt) in which the load voltage is zero due to the inductive element connected to the grid.

Note: Grid voltage is equal to: $v_g(t) = \sqrt{2}V_g sin(\omega_g t)$. Thyristors T_1 and T_4 have the same gate-signal ($\alpha_{1,4}$) whereas thyristors T_2 and T_3 also share the same gate-signal ($\alpha_{2,3}$) but phase shifted by 180^0 from $\alpha_{1,4}$.

(20 Marks)

Question 5

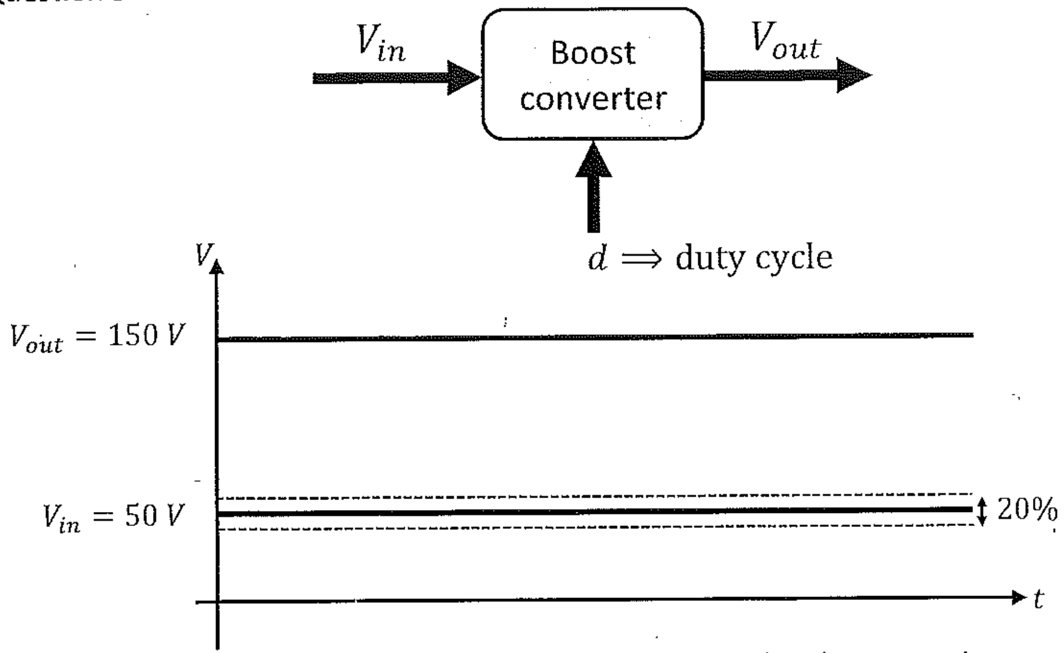

Figure Q5: Boost converter with a regulated output voltage

As shown in figure Q5 a boost converter operates on the Continuous Conduction Mode (CCM) with a input voltage of 50 V, output voltage of 150 V, switching frequency of 50 kHz, inductance of 1 mH, load resistance of 20 Ω and capacitor of 4000 μF. Determine the following if the goal is to keep the output voltage regulated at 150 V:

a) the duty cycle range if the input voltage fluctuates 20% around 50 V (as shown in figure Q5) and

b) the duty cycle range if the load is changed from 20 Ω to 40 Ω with $V_{in} = 50\ V$.

(20 Marks)

Question 6

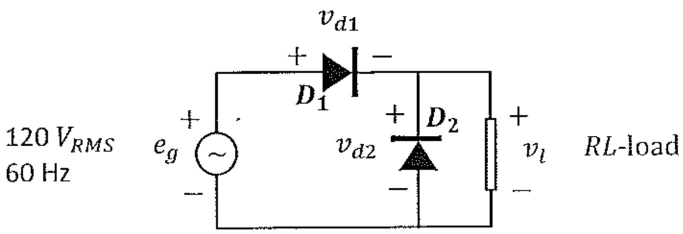

Figure Q6: Half-wave rectifier circuit without negative voltage

As shown in figure Q6 in addition to the diode D_1 an anti-parallel diode D_2 connected to the load. The diode D_2 is also known as a free-wheeling diode.

a) Assuming ideal diodes, derive expressions for the diode average voltages (V_{d1} and V_{d2}) as a function of the load power factor and amplitude of the grid voltage. Note that $V_{d1} = \langle v_{d1} \rangle$ and $V_{d2} = \langle v_{d2} \rangle$.

b) Considering a diode drop voltage equal 1 V (when it is on) for both diodes, derive an expression for the load average voltage. Consider that the RL load in figure Q6 phase shift the current by 45^0 with respect to the voltage.

(20 Marks)

Question 7

The single-phase AC voltage controller has a 230 V_{rms}, 60 Hz AC source. The normalized plot of $V_{0,rms}$ as a function of firing delay angle α is shown in figure Q7. If the load resistance is 25 Ω, determine the following:

a) the delay angle required to deliver 650 W to the load

b) the rms source current

c) the rms and average current in the SCRs

d) the power factor

e) the THD of the source current

f) roughly sketch the waveforms (source voltage, output voltage and output current) of single-phase AC voltage controller with R-L load if the delay angle α is 45^0.

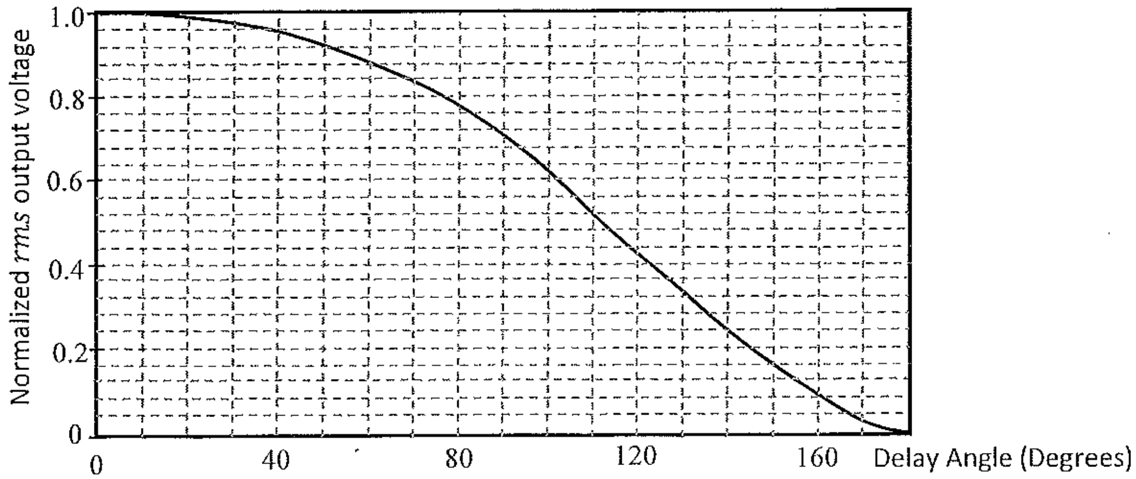

Figure Q7: Normalized rms output voltage versus firing delay angle for a single-phase AC voltage controller with a resistive load

(20 Marks)

END OF THE PAPER