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The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX5536/ECX5236 Computer architecture**
Academic Year	: 2019/20
Date	: 16th October 2020
Time	: 0930-1230hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Eight (8)** questions in **Five (5)** pages.
3. Answer any **Five (5)** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. This is a Closed Book Test (CBT).
6. Answers should be in clear hand writing.
7. Do not use Red colour pen.

1. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.
   (i) How many bits are there in the operation code, the register code part, and the address part? **[03 marks]**
   (ii) Draw the instruction word format and indicate the number of bits in each part. **[05 marks]**
   (iii) How many bits are there in the data and address inputs of the memory? **[02 marks]**
   (iv) Suppose you are designing a computer from scratch and that your company's budget allows a very small amount of memory bandwidth. Which of the following characteristics would you choose in the ISA and the microarchitecture, and why? Explain briefly. **[5 × 2 = 10 marks]**
      a) Variable length instructions or fixed length instructions?
      b) Complex instructions or simple instructions?
      c) A large L2 cache or a small L2 cache? (L2 is the last-level cache)
      d) An aggressive prefetcher or a conservative prefetcher?
      e) Large cache blocks vs. small cache blocks?

2. Your job is to evaluate the potential performance of two processors, each implementing a different ISA. The evaluation is based on its performance on a particular benchmark. On the processor implementing ISA A, the best compiled code for this benchmark performs at the rate of 10 IPC. That processor has a 500 MHz clock. On the processor implementing ISA B, the best compiled code for this benchmark performs at the rate of 2 IPC. That processor has a 600 MHz clock.
   (i) What is the performance in MIPS (millions of instruction per second) of the processor implementing ISA A? **[04 marks]**
   (ii) What is the performance in MIPS (millions of instruction per second) of the processor implementing ISA B? **[04 marks]**
   (iii) Which is the higher performance processor? Explain. **[06 marks]**
   (iv) Which is better? More RAM or a faster processor? Point out the reasons to support your answer. Answer should be in point form. **[06 marks]**

3.
   (i) Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks. **[06 marks]**
   (ii) Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline. **[06 marks]**
   (iii) A nonpipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? **[08 marks]**

4.

(i) A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word, and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instruction for this computer. **[05 marks]**

(ii) What is the difference between a microprocessor and a microprogram? Is it possible to design a microprocessor without a microprogram? **[05 marks]**

(iii) Explain the difference between hardwired control and microprogrammed control. Is it possible to have a hardwired control associated with a control memory? **[04 marks]**

(iv) The microprogrammed control organization shown in Figure 1 has the following propagation delay times. 40 ns to generate the next address, 10 ns to transfer the address into the control address register, 40 ns to access the control memory ROM, 10 ns to transfer the microinstruction into the control data register, and 40 ns to perform the required microoperations specified by the control word. What is the maximum clock frequency that the control can use? What would the clock frequency be if the control data register is not used? **[06 marks]**

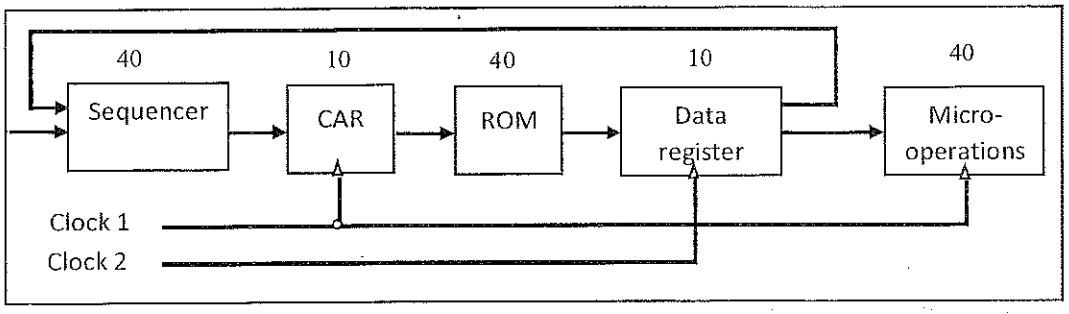

Figure 1: The microprogrammed control organization

5.

(i) Throughput of a pipeline is inversely proportional to the bottleneck of the pipeline. Explain the statement. **[05 marks]**

(ii) An instruction execution path will take 9ns to execute an instruction in one-stage pipeline. However this logic path can be divided into any number of stages and the logic delay (9ns) can be subdivided equally as well. Moreover the sum of setup time of a latch and clock skew will be 1ns. Let s as the number of stages. Assume that the pipeline receives a set of instructions without branching instructions.

a) What is the clock period T_{clock} in terms of s? **[05 marks]**

b) What is the execution time of 101 instructions? **[05 marks]**

c) Calculate the optimum number of stages that the pipeline should have for minimum execution time of 101 instructions. **[05 marks]**

6. An enhancement in a computer system improves only some part of the system. Accordingly, improvement of the performance depends on the impact of the enhancement part. The f denotes the fraction of the computational time in the old system that cannot be improved with the enhancement made; S_e is the achievable speedup only if the enhanced part of the system is used.

(i) If the old time of the system (without improvement) is T_{old} formulate the new time T_{new} of the system after the enhancement. **[05 marks]**

(ii) The speedup of the new system (after the improvement) is

$$S_{new} = \frac{T_{old}}{T_{new}}$$

Accordingly derive an equation for S_{new} in terms of f, S_e, which is Amdahl's law. **[07 marks]**

(iii) Suppose that we are considering an enhancement to the processor of a server system used for Web serving. The new CPU is 10 times faster on computation in the Web serving application than the original processor. Assuming that the original CPU is busy with computation 40% of the time and is waiting for I/O 60% of the time, what is the overall speedup (S_{new}) gained by incorporating the enhancement? **[08 marks]**

7. Assume that we have a byte-addressable toy computer that has a physical address space of 512 bytes. The computer uses a simple, one-level virtual memory system. The page table is always in physical memory. The page size is specified as 8 bytes and the virtual address space is 2 KB.

(i) How many bits of each virtual address is the virtual page number? **[02 marks]**

(ii) How many bits of each physical address is the physical frame number? **[02 marks]**

(iii) We would like to add a 128-byte write-through cache to enhance the performance of this computer. However, we would like the cache access and address translation to be performed simultaneously. In other words, we would like to index our cache using a virtual address, but do the tag comparison using the physical addresses (virtually-indexed physically-tagged). The cache we would like to add is direct-mapped, and has a block size of 2 bytes. The replacement policy is LRU (Least Recently Used). Answer the following questions:

a) How many bits of a virtual address are used to determine which byte in a block is accessed? **[02 marks]**

b) How many bits of a virtual address are used to index into the cache? Which bits exactly? **[03 marks]**

c) How many bits of the virtual page number are used to index into the cache? **[03 marks]**

d) What is the size of the tag store in bits? Show your work. **[03 marks]**

(iv) What is meant by a page fault in virtual memory organization? When a page fault occurs describe what the computer system would do? **[05 marks]**

8. A magnetic disk system has the following parameters:

T_s = average time to position the magnetic head over a track
R = rotation speed of disk in revolutions per second
N_t = number of bits per track
N_s = number of bits per sector

(i) Define the terms seek time and rotational delay. **[02 marks]**

(ii) Calculate the average time T_a that it will take to read one sector. **[05 marks]**

(iii) What is the transfer rate of an eight-track magnetic tape whose speed is 120 centimeters per second and whose density is 1600 bits per centimeter? **[05 marks]**

(iv) Specification of a hard disk of 1.2 GB made up with several platters is given as follows: 620 cylinders, 64 heads, and 63 sectors. The performance measuring utility shows the average seek time as 9ms. Disk rotational speed is calculated as 7200 rpm.

a) Calculate the average rotational delay. **[03 marks]**

b) Calculate the number of bytes in a sector of the hard disk. (Note: bytes in a sector should be the nearest to the power of two value) **[05 marks]**