The Open University of Sri Lanka

Faculty of Engineering Technology

Department of Electrical & Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX3351 / EEX3350 / ECX3150 Electronics I**
Academic Year	: 2019/2020
Date	: 4th October 2020
Time	: 1330-1630hrs
Duration	**: 3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.

2. This question paper consists of **Eight (8)** questions in **Seven (7)** pages.

3. Answer any **Five (5)** questions only. All questions carry equal marks.

4. Answer for each question should commence from a new page.

5. Relevant charts / codes are provided.

6. This is a Closed Book Test **(CBT)**.

7. Answers should be in clear hand writing.

8. Do not use red colour pens.

Q1. (a) Considering the behavior of the P-N junction in reverse and forward biased modes
derive the characteristic curve of a practical diode. **(4 Marks)**

(b) Consider the circuit in Figure-Q1 where Z is a Zenner diode with a breakdown
voltage of 5.7V and a D near-ideal Si diode with a forward voltage drop of 0.7V.
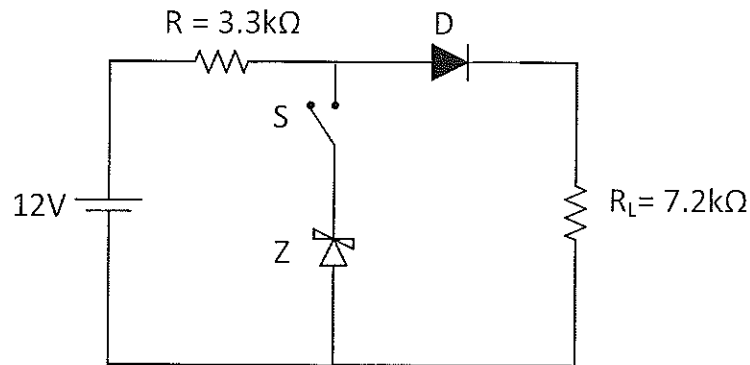
Figure-Q1

i. Let switch (S) be open initially. Calculate the voltage across the load resistance
R_L. **(4 marks)**
ii. Calculate the voltage across load resistance R_L when S is closed. **(4 marks)**
iii. Calculate the current through R_L when S is closed. **(2 marks)**
iv. Hence calculate the current flowing through the Zenner diode. **(6 marks)**

Q2. Figure-Q2 shows a temperature control system using a cooling fan. Fan motor (M) is
"ON" when the temperature rises above a threshold and it is "OFF" at low temperatures
below the threshold. Let us neglect the inductance effects of the fan motor and assume its
resistance to be 100Ω. A thermistor (T) serves as the temperature sensing element which
decreases its resistance when the temperature is increased and vise-versa. Q is a Silicone
transistor having $\beta = 100$.
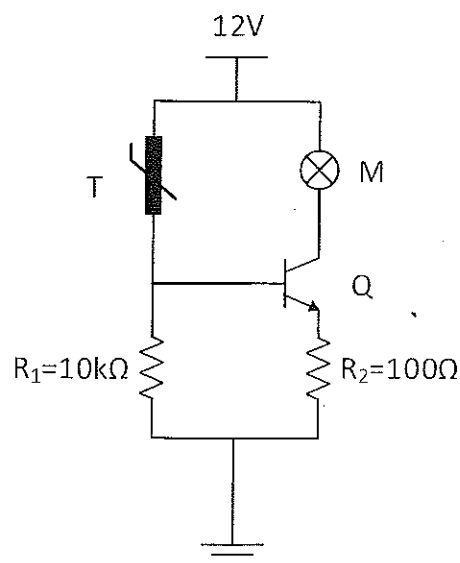
Figure-Q2

(a) What is the bias configuration used in this circuit. **(1 Mark)**

(b) Showing all your calculations fill in the Table Q2. **(9x1 Mark)**

Table-Q2

Resistance of T	V_b	I_e	I_c
100Ω			
$10k\Omega$			
$50k\Omega$			

(c) If the transistor (Q) enters cut-off at a collector current of 25mA, explain the switching operation of this circuit. **(4 Marks)**

(d) Draw a DC load line and mark the cutoff region. Hence find the range of V_{ce} during cut-off. **(6 Marks)**

Q3.

(a) List two advantages of field effect transistors over bipolar junction transistors. **(2 Marks)**

(b) Using a suitable diagram, explain the operation of an n-channel JFET. **(3 Marks)**

(c) Consider the circuit in Figure-Q3.
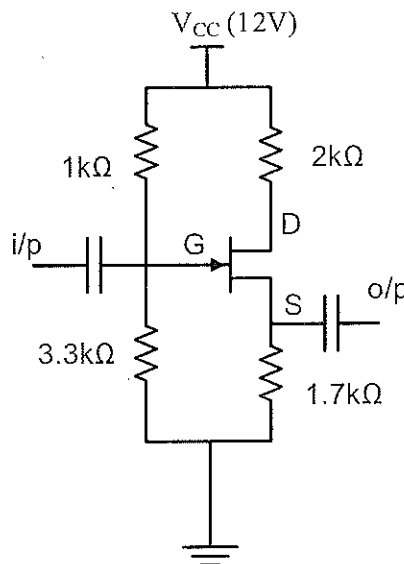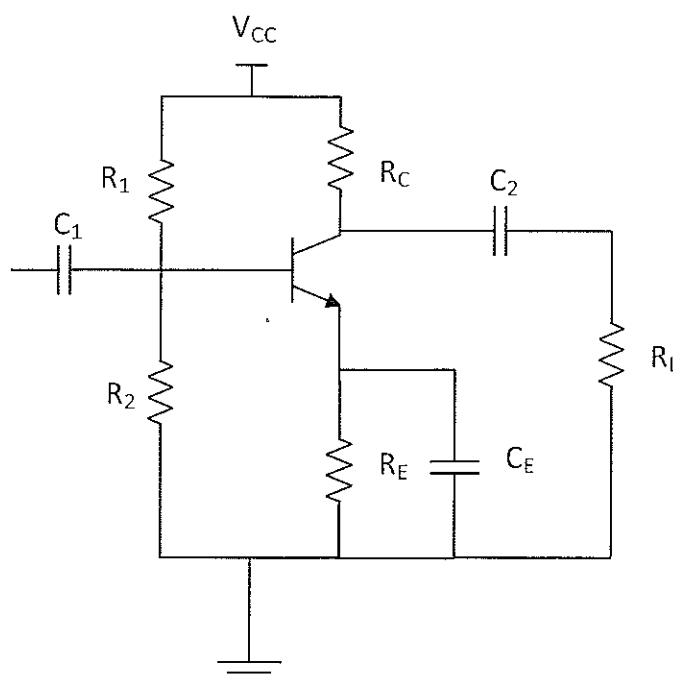

Figure-Q3

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i. What is the amplifier configuration of this circuit?   (1 Mark)
ii. Find the gate voltage, V_G.   (2 Marks)
iii. Hence find a relationship between I_D and V_{GS}.   (4 Marks)

iv. Let $V_p = -3V$ and $I_{DSS} = 12mA$. Using the square-law characteristics of the transistor
and the result in iii. find the drain current, I_D.   (8 Marks)

Q4. A small signal amplifier circuit is shown in Figure-Q4. Forward current gain (h_{fe}) and the input impedance (h_{ie}) are 50 and $1k\Omega$ respectively and neglect the effect of the h_{oe} and h_{re} of the h parameter model.
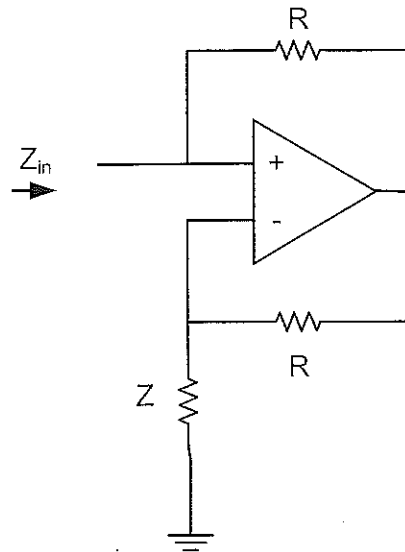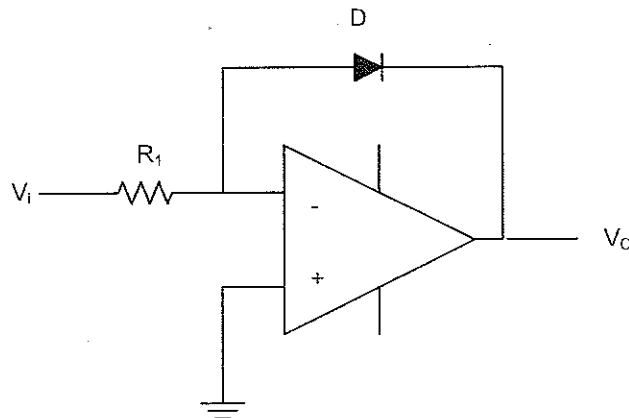

Figure-Q4

(a) Draw the AC h parameter equivalent circuit for the amplifier in FigureQ4. (5 Marks)
(b) Using above parameters, derive the expressions for the following.
    i. Current gain   (3 marks)
    ii. Voltage gain   (3 marks)
    iii. Power gain   (3 marks)
    iv. Input impedance   (3 marks)
    v. Output impedance   (3 marks)

Q5.

(a) List and explain three characteristics of an ideal operational amplifier. Discuss the deviations in practical operational amplifiers. **(3x2 Marks)**

(b) Assuming ideal operational amplifier behavior in the circuit of Figure-Q5 (a), prove that the input impedance $Z_{in} = -Z$. **(7 Marks)**

Figure –Q5 (a)

(c)

Figure-Q5 (b)

Show that the circuit in Figure-Q5 (b) can provide an input-output relationship $v_o \propto ln(v_i)$ hence this is a logarithmic amplifier. **(7 Marks)**

[**Hint**: Use the diode's characteristic equation $I_D = I_S\left(e^{\frac{v_D}{\eta V_T}} - 1\right)$]

Q6.

   (a) Perform the following conversions.
- i. 12.93_{10} to binary
- ii. 0.1_{10} to binary
- iii. 27.6_8 to hexadecimal
- iv.   -31 to 8 bit 2's complement

                                                      (4x2 Marks)

   (b) Perform the calculation 10-14 in 8 bit 2's complement arithmetic.   **(4 Marks)**

   (c) Using a truth table prove that $A\bar{B}C + AB\bar{C} + \bar{A}\bar{B}\bar{C} + AB C = A$ **(3 Marks)**

   (d) Using De Morgan's theorem prove the following.
- i. $AB + \bar{B}C = \overline{(\bar{A} + \bar{B})(B + \bar{C})}$ **(2 Marks)**
- ii. $(\bar{A} + \bar{C})(B + \bar{C})[A + B(\bar{B} + \bar{C})] = AC + \bar{B}C + \bar{A}(\bar{B} + BC)$ **(3 Marks)**

Q7. A seven segment display is a common indicator circuit used in electronic circuits. Consider the following seven segment display in Figure-Q7. The unit should display a number from 0-9 based on a binary input provided. As an example, for a binary input 0000 one should light the segments a, b, c, e, f and g only. You are required to design the seven segment driver combinational logic circuit.
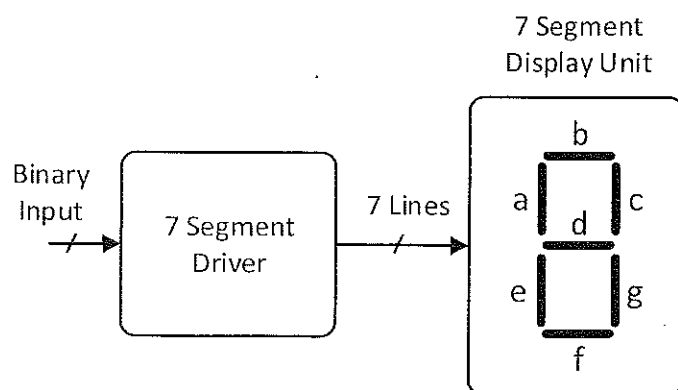
Figure-Q7

      (a) Draw a truth table indicating the 4 bit binary input and the seven segment output. Assign an "ON" segment to logic state "1".   **(6 Marks)**

      (b) Derive the simplified logic expressions using Karnaugh maps.   **(7x1 Marks)**

      (c) Implement the circuit using NAND gates.   **(7x1 Marks)**

Q8.

      (a) A three variable Boolean expression is given by $F = \prod M(1,2,4,5)$. Using Karnaugh maps find,
- i.   minimum POS and
- ii.   minimum SOP.

                                                       (2x5 Marks)

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(b) A certain synchronous up-counter circuit outputs a sequence 0, 3, 6, 9, 12, 15, 0 ,....You are required to design a sequential logic circuit consisting of J-K flip flops and common logic gates.

    i.   Determine the number of J-K flip flops required for this circuit.   **(1 Mark)**

    ii.   Draw the state diagram.   **(3 Marks)**

    iii.   Deduce the state table.   **(6 Marks)**