00080

The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Codes and Title	**: EEX4350/ECX4150 ELECTRONICS II**
Academic Year	: 2019/20
Date	: 06th October 2020
Time	: 13:30-16:30hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This is a Closed Book Test (CBT).
3. This question paper consists of **eight (08)** questions in **four (04)** pages.
4. Relevant data sheets are provided separately in pages 5-9.
5. Answer five (05) questions only. All questions carry equal marks.
6. Calculators are permitted to use.
7. Relevant data sheets/information are provided.
8. Do not use Red colour pen.

Question 1

a) Explain how the propagation delays of gates in a digital circuit affects the performance. (05 marks)

b) Draw the state diagram of a sequence detector to detect the non-overlapping binary sequence 10111. (05 marks)

c) In a network, eight (08) input bit streams need to be interfaced to a parallel printer buffer. At a given time, only one bit stream is interfaced to the buffer. Each input bit stream is given a token with decimal numbers 1 to 8 with decreasing priority in the increasing order of the token value. The token 1 has the highest priority while the token number 8 has the lowest priority. Draw the schematic of the digital circuit using 74LS148 a 8:3 priority encoder and 74HCT1284 printer buffer ICs.
Data sheets are provided for 74LS148 and 74HCT1284 your reference. (10 marks)

Question 2

a) Describe two applications of oscillators in communication systems. (04 marks)

b) Consider a digital circuit which has an input A = 0 0 1 0 1 1 0 1 0 1 1 to give an output Y=1 when the input bit sequences 1101 or 011 are detected. Draw the state diagram for the above logic operations. (06 marks)

c) Design a digital circuit using the SN74LS02 and SN74LS03 ICs shown below to realize the Boolean function F(X,Y,Z) = (XZ + YX)(X+Y). Clearly state any assumptions you make in the design. Relevant data sheets with pin diagrams are attached herewith. (10 marks)

Question 3

a) List three different coupling mechanisms used in multi-stage cascaded bipolar junction transistor amplifier systems. (03 marks)

b) In a 'n'-stage cascaded amplifier system there are 'n' different amplifiers connected such that the output of one stage is fed as the input of the next stage. Derive an expression to compute the overall voltage gain of this cascaded system. (07 marks)

c) Derive an expression for stability, S = dIc/dIco, Ic denotes the collector current and Ico denotes the reverse saturation current for the fixed bias circuit shown in Figure 1. (10 marks)

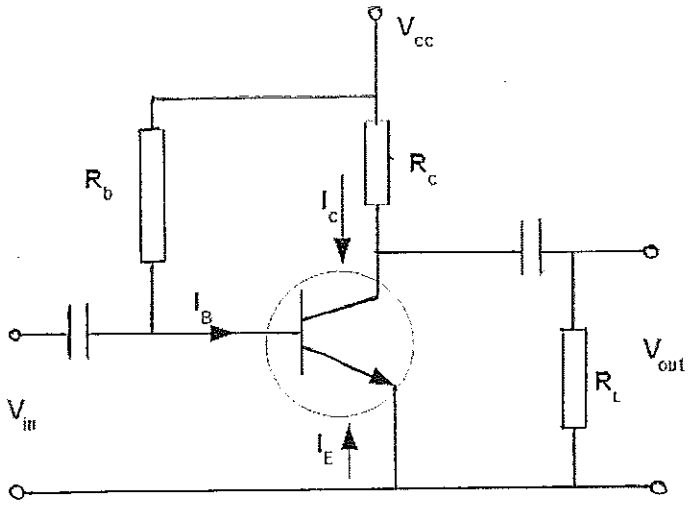


Figure 1

Question 4

a) Explain the operation of an astable multivibrator using a suitable circuit using an operational amplifier.
Clearly state any assumptions you make in your answer. (05 marks)

b) Compare the operation of ClassA, Class B and Class C power amplifiers. (05 marks)

c) Verify whether the circuit shown in Figure 2, to measure a DC current in the range of 0 mA to 1 mA using an ammeter which has a sensitivity range of 0 mA to 10 mA will operate satisfactorily. The internal resistance (Rs) of the ammeter is 150Ω. (10 marks)

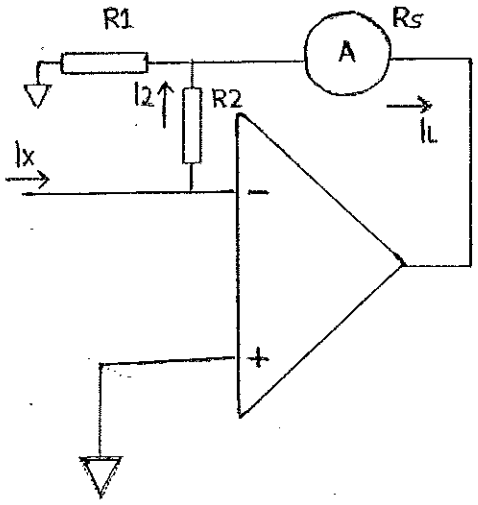


Figure 2

Question 5

a) Draw the input and output voltage variations over time of a Schmitt trigger. (06 marks)

b) Consider the ideal integrator circuit shown in Figure 3.

i. Input voltage is a sinusoid of the form $v_{in} = A\,sint(\omega t)$ V. Derive an expression to compute the output voltage of the integrator. (10 marks)

ii. If $v_{in} = 0.8\,sint(100t)$V, calculate the peak output voltage value when Rx = Ry = 100kΩ and C=1μF (Figure 3). (04 marks)

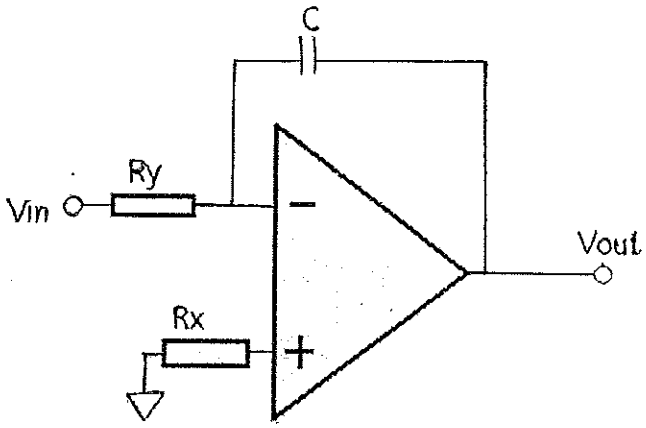


Figure 3

Question 6

a) Considering the typical frequency response of the open loop gain (A) of an operational amplifier define the following terms along with the appropriate equations. (06 marks)

(i) gain bandwidth product (BW)
(ii) unity gain frequency (f_u)
(iii) cut-off frequency (f_c)

b) Consider the operational amplifier circuit with a gain "A" shown in Figure 4.

i) Derive an expression which relates the input voltage (Vin) and output voltage (Vout). (08 marks)

ii) Find the closed loop gain where Rin is 15 kΩ and Rf is 100 kΩ. (03 marks)

iii) Calculate the output voltage Vout when Vin is 2.5V r.m.s. (03 marks)

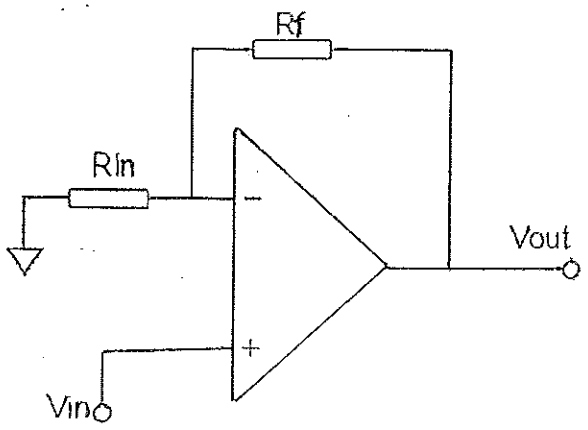


Figure 4

Question 7

a) Describe two applications of filters in communication systems. (06 marks)

b) Consider a Wein bridge oscillator shown in Figure 5 with Z1 is a series resistor capacitor (RC) combination ($Z1 = R1\text{-}jX_{c1}$) and Z2 as a parallel RC combination ($Z2 = R2 \parallel C2$).

(i) Derive an expression for the oscillation frequency. Clearly state any assumptions you make in your answer. (10 marks)

(ii) Determine the feedback ratio at the oscillation frequency if the resistors and capacitor values of Z1 and Z2 are equal and represented as R and C. (04 marks)

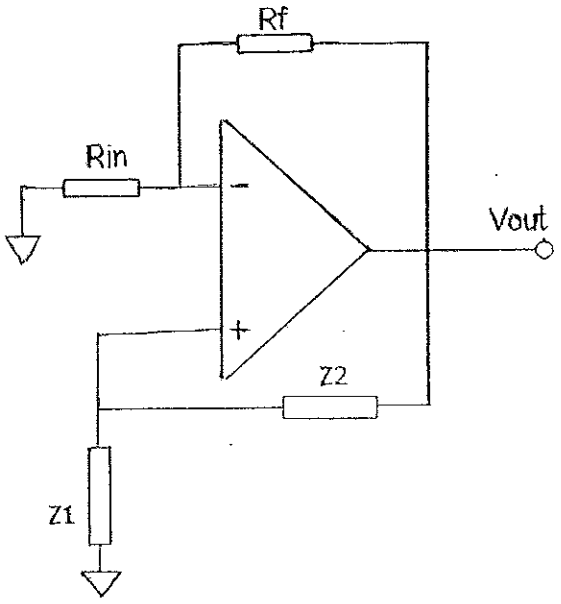


Figure 5

Question 8

a) Explain the structure and operation of a diac with V-I characteristics, relevant notations and schematic diagrams. (10 marks)

b) Consider an emitter follower circuit with a p-n-p transistor. Other components in the circuit include an input coupling capacitor 'C1', biasing resistor pair 'R1' and 'R2', input voltage 'Vs' with source resistance 'Rs' and DC biasing voltage 'Vcc'.

(i) Draw the circuit diagram. (05 marks)

(ii) Derive an expression for the voltage gain of this circuit considering the h-parameters when the load resistance is infinite. (05 marks)

SDLS028

SN5403, SN54LS03, SN54S03, SN7403, SN74LS03, SN74S03
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

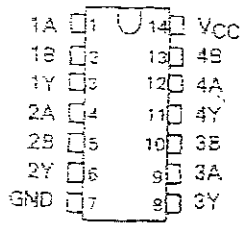
These devices contain four independent 2-input NAND gates. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN5403, SN54LS03 and SN54S03 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7403, SN74LS03 and SN74S03 are characterized for operation from 0°C to 70°C.

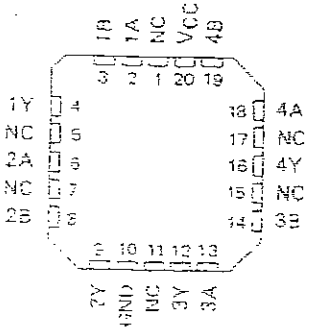
FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN5403 . . . J OR W PACKAGE
SN54LS03, SN54S03 . . . J OR W PACKAGE
SN7403 . . . N PACKAGE
SN74LS03, SN74S03 . . . D OR N PACKAGE
(TOP VIEW)

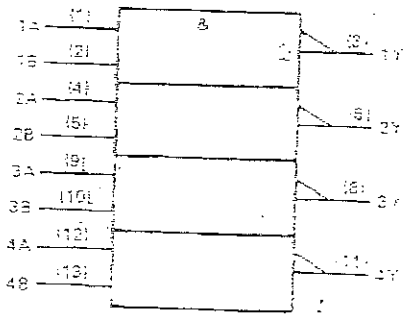


SN54LS03, SN54S03 . . . FK PACKAGE
(TOP VIEW)



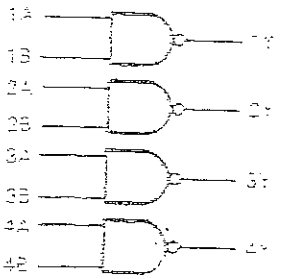
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



$Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

SDLS027

SN5402, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

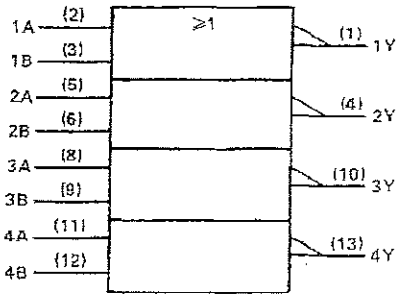
These devices contain four independent 2-input NOR gates.

The SN5402, SN54LS02, and SN54S02 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7402, SN74LS02, and SN74S02 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

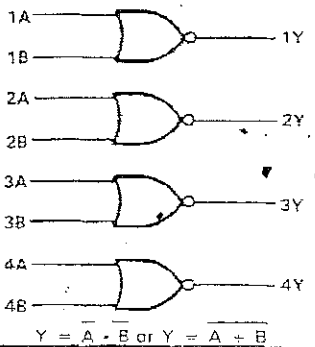
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†



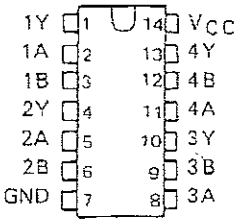
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

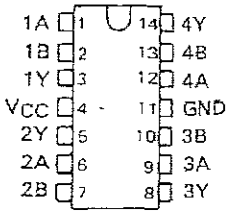


$Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$

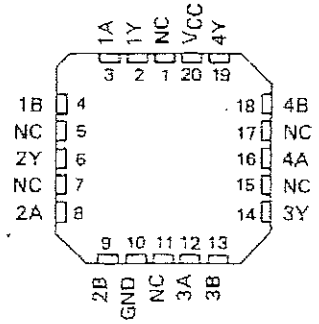
SN5402 . . . J PACKAGE
SN54LS02, SN54S02 . . . J OR W PACKAGE
SN7402 . . . N PACKAGE
SN74LS02, SN74S02 . . . D OR N PACKAGE
(TOP VIEW)



SN5402 . . . W PACKAGE
(TOP VIEW)



SN54LS02, SN54S02 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

Parallel printer interface transceiver/buffer

74HCT1284

FEATURES

- Asynchronous operation
- 4-Bit transceivers
- 3 additional buffer/driver lines
- TTL compatible inputs
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Input Hysteresis
- Low Noise Operation
- Center Pin V_{CC} & GND
- IEEE 1284 Compliant Level 1 & 2
- Overvoltage Protection on B side

DESCRIPTION

The 74HCT1284 parallel interface chip is designed to provide an asynchronous, 4-bit, bi-directional, parallel printer interface for personal computers. Three additional lines are included to provide handshaking signals between the host and the peripheral. The part is designed to match IEEE 1284 standard.

The 4 transceiver pins (A/B 1-4) allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending on the state of the direction pin DIR.

The B bus and the Y5-Y7 lines have totem pole or open drain style outputs depending on the state of the high drive enable pin HD. The A bus only has totem pole style outputs. All inputs are TTL compatible with at least 400mV of input hysteresis at V_{CC} = 5.0V.

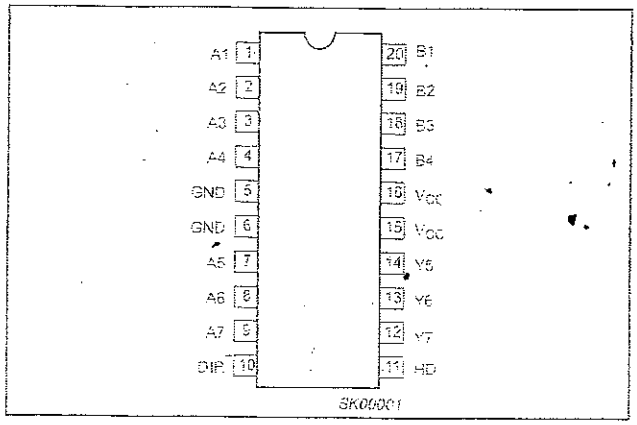
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay Bn to An	C_L = 50pF; V_{CC} = 5V	5.3 5.6	ns ns
C_{IN}	Input capacitance A_n, DIR, HD	V_I = 0V or V_{CC}	5	pF
C_{OUT}	Output capacitance B_n, Y_n	V_O = 0V or V_{CC}; 3-State	14	pF
I_{CC}	Total supply current	V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic DIP	0°C to +70°C	74HCT1284N	SOT146-1
20-pin plastic SOL	0°C to +70°C	7HCT1284D	SOT163-1
20-pin plastic SSOP Type II	0°C to +70°C	74HCT1284DB	SOT339-1
20-pin plastic TSSOP Type I	0°C to +70°C	74HCT1284PW	SOT360-1

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1,2,3,4 20,19,18,17	A1 - A4 B1 - B4	Data inputs/outputs
7,8,9 14,13,12	A5 - A7 Y5 - Y7	Buffer/Driver lines
10,11	DIR,HIGH DRIVE	Direction, Drive
5,6	GND	Ground (0V)
15,16	V_{CC}	Positive supply voltage

MOTOROLA

10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

SN54/74LS147
SN54/74LS148
SN54/74LS748

10-LINE-TO-4-LINE
AND 8-LINE-TO-3-LINE
PRIORITY ENCODERS

LOW POWER SCHOTTKY

The SN54/74LS147 and the SN54/74LS148 are Priority Encoders. They provide priority decoding of the inputs to ensure that only the highest order data line is encoded. Both devices have data inputs and outputs which are active at the low logic level.

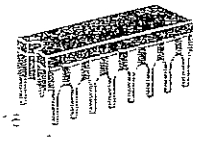
The LS147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition does not require an input condition because zero is encoded when all nine data lines are at a high logic level.

The LS148 encodes eight data lines to three-line (4-2-1) binary (octal). By providing cascading circuitry (Enable Input EI and Enable Output EO) octal expansion is allowed without needing external circuitry.

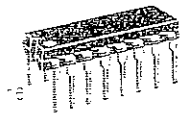
The SN54/74LS748 is a proprietary Motorola part incorporating a built-in deglitcher network which minimizes glitches on the GS output. The glitch occurs on the negative going transition of the EI input when data inputs 0–7 are at logical ones.

The only dc parameter differences between the LS148 and the LS748 are that: (1) Pin 10 (input 0) has a fan-in of 2 on the LS748 versus a fan-in of 1 on the LS148; (2) Pins 1, 2, 3, 4, 11, 12 and 13 (inputs 1, 2, 3, 4, 5, 6, 7) have a fan-in of 3 on the LS748 versus a fan-in of 2 on the LS148.

The only ac difference is that tPHL from EI to EO is changed from 40 to 45 ns.



J SUFFIX
CERAMIC
CASE 620-09



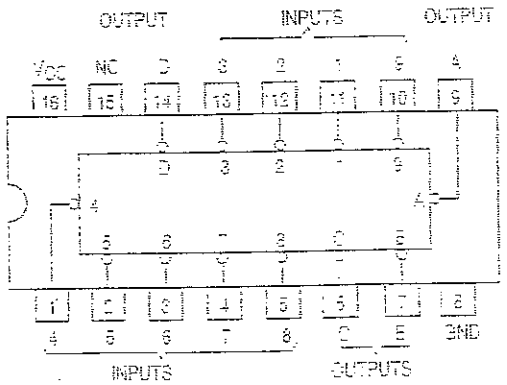
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

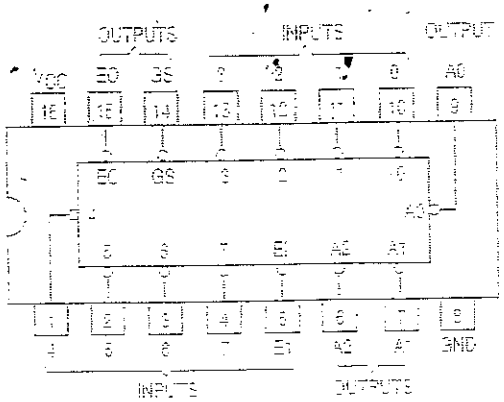
ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

SN54/74LS147
(TOP VIEW)



SN54/74LS148
SN54/74LS748
(TOP VIEW)



SN54/74LS147 • SN54/74LS148 • SN54/74LS748

SN54/74LS147
FUNCTION TABLE

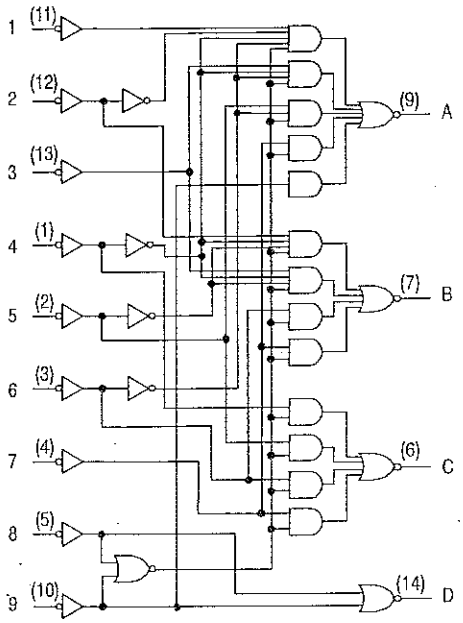
INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Logic Level, L = LOW Logic Level, X = Irrelevant

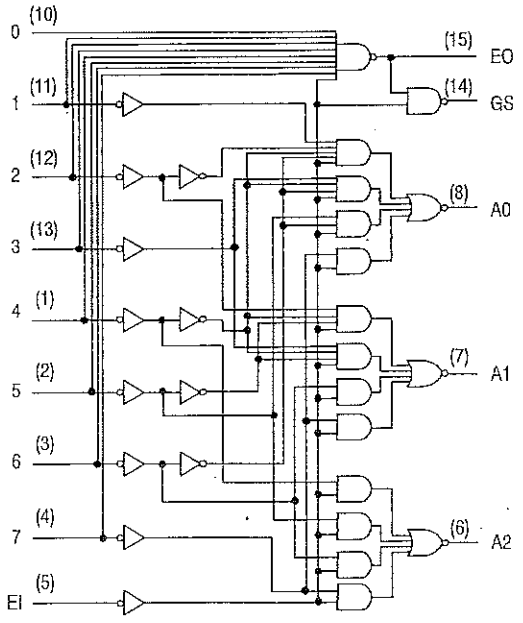
SN54/74LS148
SN54/74LS748
FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

FUNCTIONAL BLOCK DIAGRAMS



SN54/74LS147



SN54/74LS148