The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX4530/EEX4230- Fault Diagnosis in Electronic Circuits**
Academic Year	: 2019/2020
Date	: 29th September 2020
Time	: 1330-1630hrs

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of Eight **(8)** questions in **Nine (09)** pages.
3. Answer any **Five (5)** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. This is a Closed Book Test (CBT).
6. Answers should be in clear hand writing.
7. **Do not** use a red colour pen.
8. Adhere to usual notations.

1. A single-stage transistor amplifier (Collector to Base bias) is shown in Figure 1. The current gain of the transistor is 50.

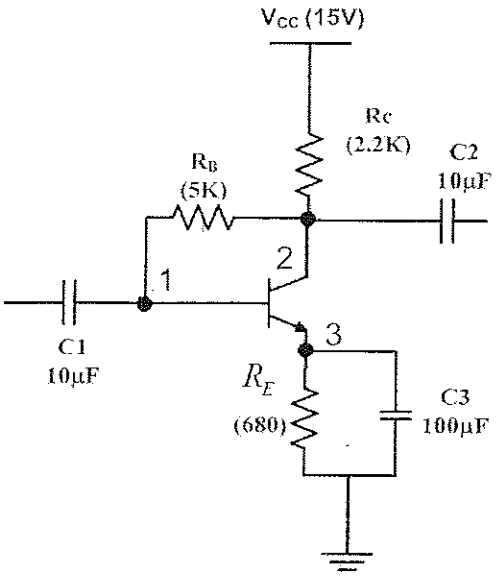

Figure 1

a. Calculate the voltages of test point 1, 2 and 3 at no signal condition. [06 Marks]

b. The table given below shows the voltages at test points under faulty conditions. Find the faulty components and the type of faults by giving reasons. [08 Marks]

Case	TP1 (V)	TP2(V)	TP3(V)	Symptom
A	15	15	14.3	No output
B	0	15	0	No output
C	1.9	11	1.2	No output
D	3.9	4.4	3.2	Low Gain

c. Calculate the test point voltages, when BE is short circuited. [06 Marks]

2. A single stage amplifier circuit is shown in Figure 2. I_{DSS} =10mA, and $V_{GS\,(off)}$ = -3V.

a. Calculate,

i. Gate voltage [02 Marks]

ii. Drain current [04 Marks]

iii. Gate source voltage [02 Marks]

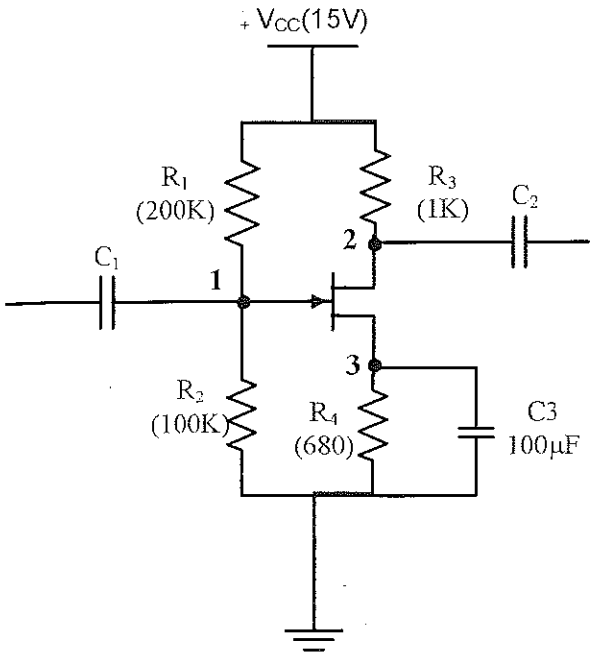

Figure 2

b. Calculate the test point voltages at no signal. [03 Marks]

c. Find the type of fault with the faulty component/s in each case giving reasons. [09 Marks]

Case	TP 1(V)	TP 2(V)	TP 3(V)	Symptom
A	5	3.91	6.81	Low gain
B	5	15	0	No output
C	5	3.91	6.81	No output

3.

a. After repairing a DC power supply, what are the parameters you should check to confirm its correct operation. [03 Marks]

b. The circuit of a DC power supply is shown in Figure 3. Assume the voltage at test point 1 lies between 12V to 15V.

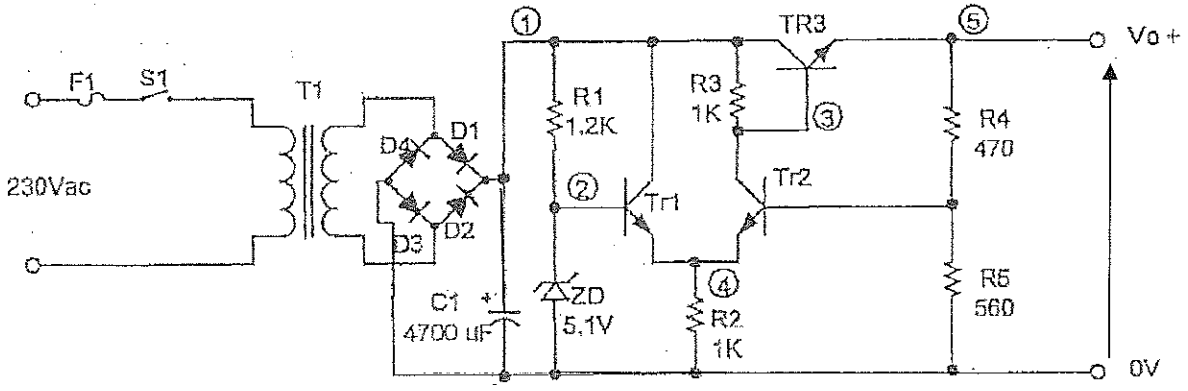

Figure 3

i. Calculate the output voltage (V_o) [03 Marks]

ii. Show a method to obtain any voltage between 5V to 10V.
State any assumptions that you made. [02 Marks]

iii. Show how you modify the given circuit to limit the current flow, if the maximum load current is 2A. [03 Marks]

iv. The table below shows the voltages at test points under fault conditions. Find the faulty component/s and fault type giving reasons. [09 Marks]

Case	TP1	TP2	TP3	TP4	TP5
A	15.0	5.1	14.7	4.5	14.0
B	15.0	5.1	15.0	4.5	0
C	15.0	5.1	5.7	4.5	5.1

4. A DC amplifier circuit is shown in Figure 4.

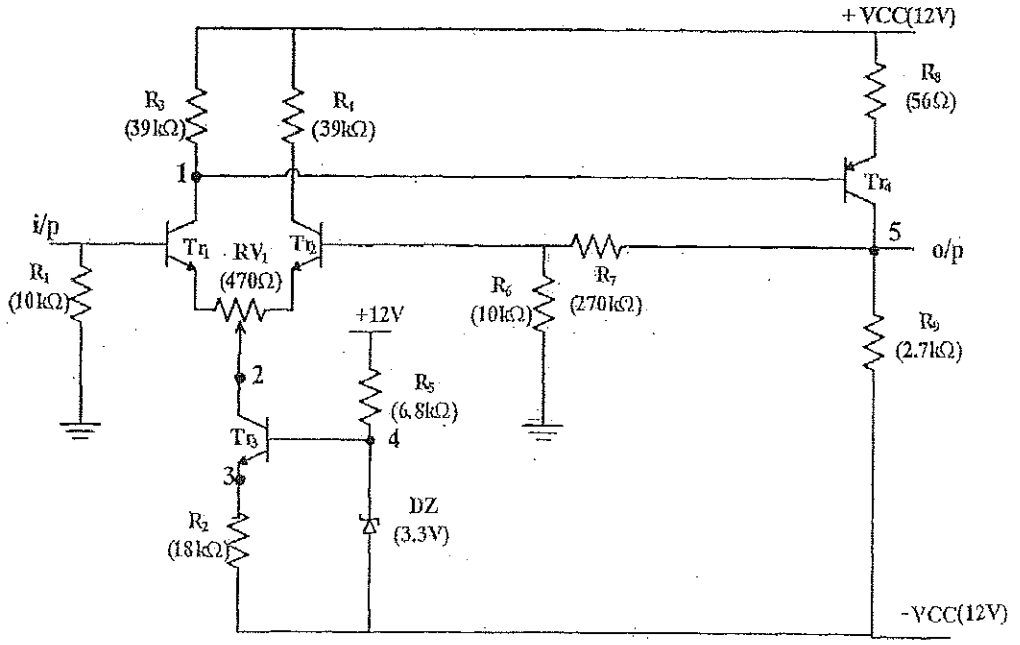

Figure 4

a. Write the type of the feedback used in this amplifier circuit and give the path of the feedback. [02 Marks]

b. Calculate the test point voltages at no signal. (Assume that Tr1 and Tr2 are matched pair of transistors) [08 Marks]

c. Calculate the voltage gain of this circuit. [02 Marks]

d. Find the fault component/s giving reasons. [08 Marks]

Fault	TP1	TP2	TP3	TP4	TP5
P	11.9	-0.9	-9.3	-8.7	-12.0
Q	12.0	5.6	5.8	6.4	-12.0
R	11.8	-0.9	-9.3	-8.7	-12.0
S	11.4	-0.9	-9.3	-8.7	-12.0

5.

a. An amplifier of open loop A_0 is supplied with positive feedback. If the feedback ratio is β, find an expression for the overall gain. [02 Marks]

b. What will happen when $\beta A_0 = 1$? [02 Marks]

c. The circuit shown in Figure 5 is a blocking oscillator.

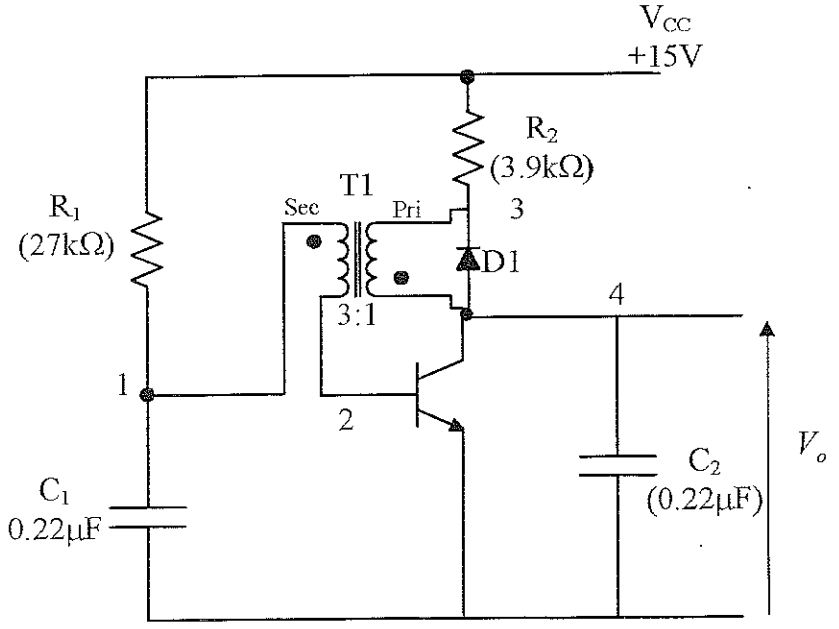

Figure 5

i. When the transistor is switched on, sketch the wave forms $V_{34,}$, V_2 and V_4 on a common time scale for two cycles. [06 Marks]

ii. Estimate the approximate lowest frequency of the output signal. [02 Marks]

iii. State the faulty component/s and fault type with reasons for the following.

A. If the oscillator produces negative going pulses of short period [02 Marks]

B. If the frequency of oscillation is correct but the amplitude of the output pulse is small. [02 Marks]

C. If the observed voltages of the test points are, [04 Marks]

Fault	TP 1	TP 2	TP 3	TP 4	Symptom
A	0.7	0.7	0.4	0.2	No Output
B	0.7	0.7	15	15	No Output

6.

a. Draw a basic block diagram of an oscillator circuit. [02 Marks]

b. State the factors that are causing frequency instability in the oscillator. Explain how you are going to eliminate those effects. [04 Marks]

c. Figure 6 shows a Wien bridge oscillator circuit. Transistors used in the Figure 6 have high current gains.

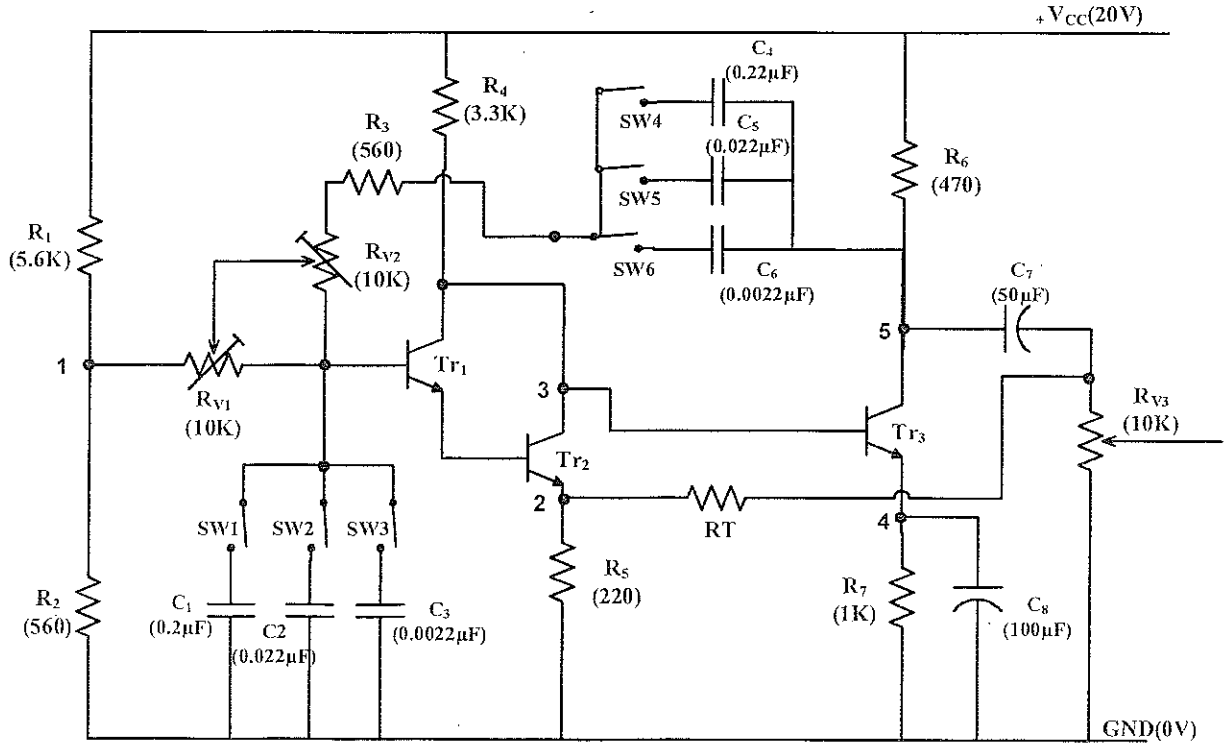

Figure 6

i. Calculate the possible output frequency ranges in this circuit. [01 Marks]

ii. Calculate the test point voltages shown in Figure 6 (State necessary assumptions). [04 Marks]

iii. Find the fault and the faulty components for the following cases. [09 Marks]

Case	TP1	TP2	TP3	TP4	TP5	Symptom/s
A	1.8	0.1	18.8	18.2	18.3	No output
B	1.8	0.6	10.6	10.0	15.2	No output with the change in switching position
C	10.7	9.5	9.6	9.0	9.1	No output

7. Consider the multivibrator circuit shown in Figure 7.The transistors may be assumed as high gain and $V_{CE}(sat) = 0$.

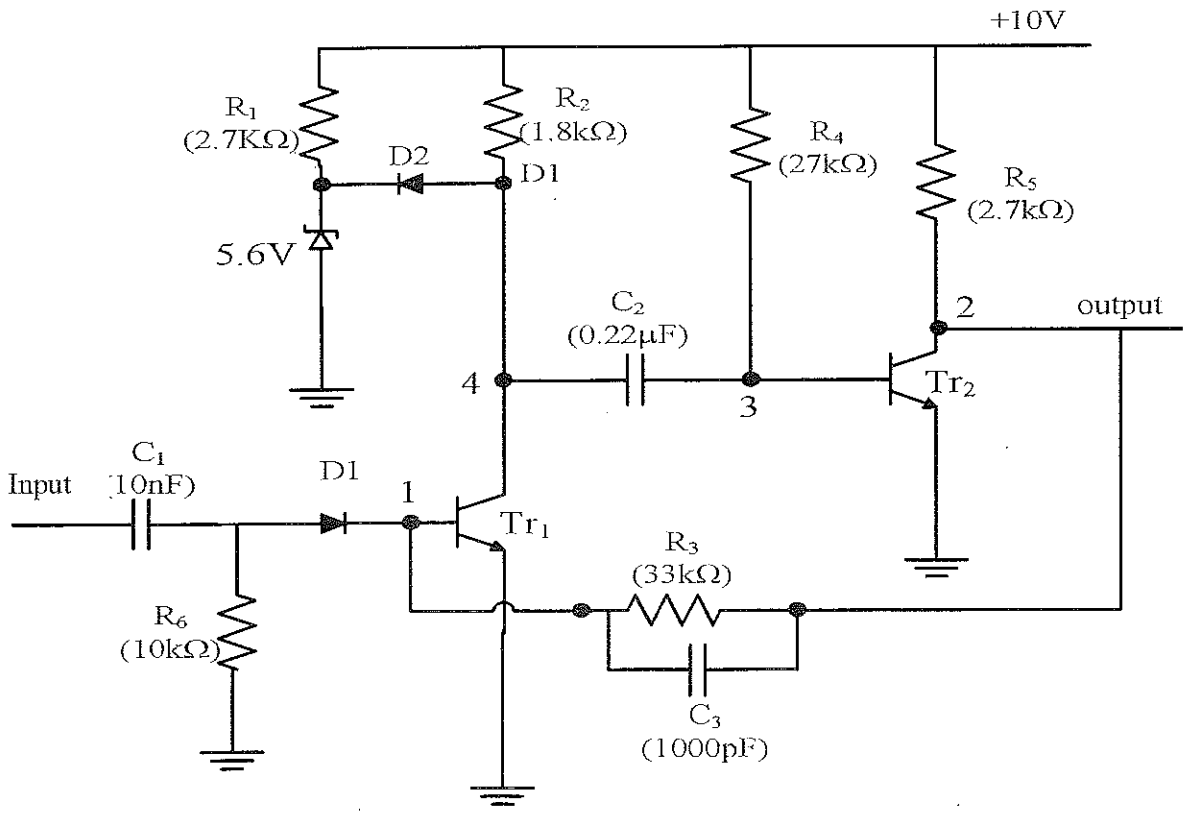

Figure 7

a. By giving reasons, identify the type of the type of the multivibrator shown in figure 07. [01 Marks]

b. Calculate the test point voltages when there is no input signal and find the collector current in each transistor. [05 Marks]

c. A pulse train of short duration having amplitude of 8V is applied to the input. Draw the resulting waveforms at each test point on a common time scale. Calculate and mark important voltage and time values on your sketch. [06 Marks]

d. Under fault conditions, all test point voltages are observed before applying any input. Then the test points are observed by an oscilloscope after applying narrow test pulse of 8V. Some of the results observed are listed below. Find the faulty component/s indicating the fault type with reasons. [08 Marks]

Case	TP1	TP2	TP3	TP4	Symptom/s
A	0.0	0.0	0.7	0.7	No output
B	0.0	0.0	0.7	6.2	No output pulse; negative pulse at **TP3**
C	0.0	0.0	0.7	6.2	Output pulse width> Normal
D	0.0	0.0	0.7	6.2	Output pulse height> Normal

8. Two Logic circuits are shown in Figure 8.

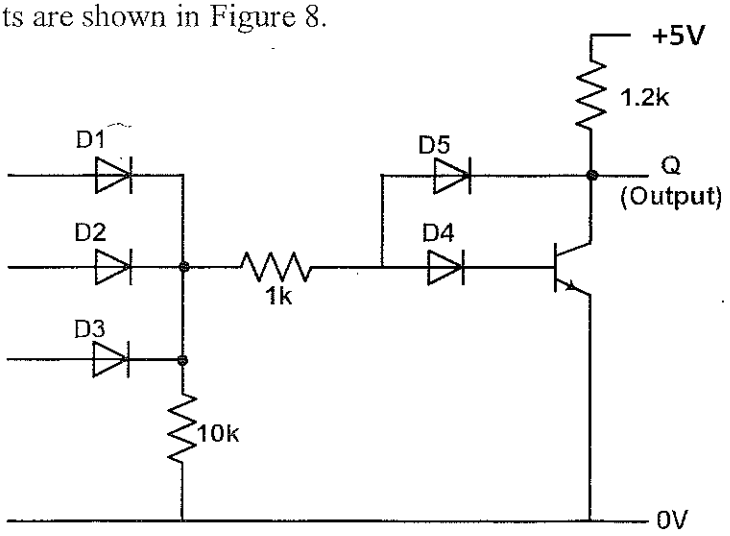

Figure 8-(a)

a) For the circuit shown in Figure 8 (a).

i. Write the truth table for this circuit shown in figure 8-(a) [03 marks]

ii. State the logic function of the circuit. [01 mark]

iii. Table 8.1 shows the observations of inputs using the logic probe.

Table 8.1: Output conditions

A	B	C
No Light	**No Light**	**Light**
No Light	**Light**	**Blink**
Light	**Light**	**Blink**

Indicate the corresponding observations of the logic probe on the output (Q) for the following faults for each of the above input conditions. [06 marks]

Fault 1: D4 short circuited
Fault 2: D3 short circuited

b) Consider the logic circuit shown in Figure 8 (b).

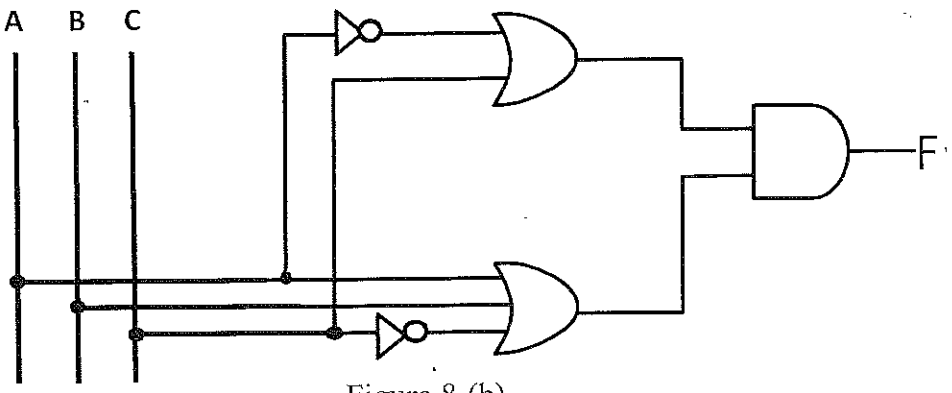

Figure 8-(b)

i. The inputs and the output of the circuit are A, B, C and F respectively. Derive a truth table to represent the 0 and 1(logic-0 and logic-1) faults at the output. The truth table should show all the inputs and the output conditions along with the response of the fault free circuit (logic 1) and the circuit with the faults (logic 0). You may assume that there is only one fault for one instance. [08 marks]

ii. Using the results in (b) (i), state the minimum number of the input combinations that detects all the faults stated above. [02 marks]

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