00036

The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX5564 Computer Organization and Operating Systems**
Academic Year	: 2020/21
Date	: 17th February 2022
Time	: 0930 - 12300 hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **seven** (7) questions on **four** (4) pages.
3. Answer any **five** questions. Each question carry equal marks.
4. The answer for each question should commence from a new page.
5. This is a Closed Book Test (CBT).
6. Answers should be in clear handwriting.
7. Do not use Red colour pen.

Question 01

a) Consider the table of processes given below. Draw Gantt charts for First Come First Served, Shortest Job Next, Non-preemptive Priority and Round Robin scheduling algorithms. Time is given in milliseconds. State all your assumptions. **[12 marks]**

Job	Arrival Time	CPU-Burst Time	Priority
P1	0	3	1
P2	0	2	3
P3	3	3	5
P4	5	5	4
P5	10	4	2
P6	12	6	1
P7	15	2	3
P8	16	4	3
P9	20	3	2
P10	22	2	2
P11	26	2	3
P12	26	6	1

b) Which scheduling algorithm gives the best turnaround time? **[08 marks]**

Question 02

Consider the following sequence of memory addresses requested by a processor during executing the particular process.

134,245,232,634,325,492,75,156,100,1045,527,483,758,823,902,45,83

a) Using the above sequence of memory addresses, prepare a reference string considering a page size is 100. **[2 marks]**

b) Using the following page replacement algorithms, find the page Hits and Page misses.

I. First in First out algorithm. **[4 marks]**

II. Optimal page algorithm. **[4 marks]**

III. Least Recently Used (LRU) algorithm. **[4 marks]**

c) Hence calculate the page miss/fault rate for each algorithm. **[6 marks]**

Question 03

You are supposed to design a new microcontroller that uses a 512K memory unit with 32bit-word of each. A binary instruction code will be stored in one word of this memory. This processor has 32 general-purpose registers, ALU and CU. The instruction used in this processor has four parts: an indirect bit, an operation code, a register code part, and an address part. Assume that the processor should perform basic operations such as Addition, Subtraction,

Multiplication, Division, Moving to a general-purpose register, Moving to an External Address, and so on.

a) How many bits are there in the operation code part, the register code part, and the address part? **[3 marks]**

b) Draw the instruction word format and indicate the number of bits in each part. **[5 marks]**

c) How many instructions can be created in the Instruction Set architecture of this processor? **[2 marks]**

d) Create the first five instructions of the Instruction set architecture specifying Instruction, Opcode, and Operand. **[10 marks]**

Question 04

Consider the scenario given in the table below, where "P" indicates a process and "R" indicates a resource.

Time	Action
1	P1 request and is allocated R1
2	P1 request R3
3	P2 request and is allocated R3
4	P2 request and is allocated R2
5	P3 request R3
6	P3 request R4
7	P4 request and is allocated R4
8	P4 request R1
9	P5 request R4
10	P5 request and allocated R5

a) Use Holt's deadlocks modelling method to analyze the above scenario. **[10 marks]**

b) Suggest a new request or request change that the system becomes deadlock in the next time stamp and show it in the resource allocation graph. **[8marks]**

c) Suggest a suitable method to eliminate the deadlock created in question 4. (b). **[2 marks]**

Question 05

A pipelined processor has a clock rate of 2.5 GHz and executes a program with 1.5 million instructions. The pipeline has five stages, and all instructions are issued at a rate of one per clock cycle. Ignore penalties due to branch instructions and out of sequence executions.

a) What is the speedup of this processor for this program compared to a nonpipelined processor, which also works at a 2.5GHz clock rate, ignoring the initial filling up of the pipeline and final emptying of it? **[10 marks]**

b) What is the throughput (in MIPS) of the pipelined processor? **[4 marks]**

c) Briefly explain Structural, Data and Control hazards in pipelined processor with appropriate examples. **[6 marks]**

Question 06

a) Consider the following Boolean expression,

A [B+C (AB+AC)]

I. Draw a logic circuit diagram for implementing it. **[5 marks]**

II. Minimize the expression using Boolean rules you learned. **[7 marks]**

III. Draw a logic circuit diagram for simplified expression. **[3 marks]**

b) Convert the following SOP (Sum of Product) expression to an equivalent POS (Product of Sum) expression. **[5 marks]**

XY+XZ+'XYZ

Question 07

A magnetic disk system has the following parameters:

Ts = average time to position the magnetic head over a track

R = rotation speed of disk in revolutions per second

Nt = number of bits per track

Ns = number of bits per sector

a) Define the terms seek time and rotational delay. **[2 marks]**

b) Using the given parameters, calculate the average time taken to read one sector. **[6 marks]**

c) The movable head disk has a rotating speed of 7500 rpm. The average seek time of the disk is 25ms, and the data transfer time is 0.00094 ms per byte. The sector size of the disk is 512 Bytes, and the number of sectors on a track is 100. Calculate the access time of a record if size of the record is 100Bytes. **[12 marks]**

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