

The Open University of Sri Lanka  
Faculty of Engineering Technology  
Department of Electrical & Computer Engineering



Study Programme	: Bachelor of Software Engineering Honours
Name of the Examination	: Final Examination
<b>Course Code and Title</b>	<b>: EEX5563/ECX5263 Computer Organization and Operating Systems</b>
Academic Year	: 2019/20
Date	: 16 <sup>th</sup> October 2020
Time	: 0930 - 1230hrs
Duration	: <b>3 hours</b>

### General Instructions

1. Read all instructions carefully before answering the questions.
  2. This question paper consists of **Eight (8)** questions in **Five (5)** pages.
  3. Answer any **Five (5)** questions only. All questions carry equal marks.
  4. Answer for each question should commence from a new page.
  5. This is a Closed Book Test (CBT).
  6. Answers should be in clear hand writing.
  7. Do not use Red colour pen.
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[ 1.]

- (a) Consider the table of processes given below. Draw Gantt charts for First Come First Served, Shortest Job Next, Non-preemptive Priority and Round Robin scheduling algorithms. Time is given in milliseconds. State all your assumptions. [12 marks]

Job	Arrival Time	CPU-Burst Time	Priority
A	0	3	4
B	0	5	1
C	0	2	3
D	6	4	2
E	15	3	3
F	16	2	5
G	16	4	2
H	27	5	4
I	27	2	5
J	27	6	2
K	32	3	1
L	34	4	3
M	35	3	4

- (b) Which scheduling algorithm gives the best turnaround time? [08 marks]

[ 2.] A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four fields: an indirect bit, an operation code, a register fields to specify one of 64 registers, and memory field.

- (a) How many bits are there in the operation code, the register code part, and the address fields? [03 marks]
- (b) Draw the instruction word format and indicate the number of bits in each part. [05 marks]
- (c) How many bits are there in the data and address inputs of the memory? [02 marks]
- (d) Suppose you are designing a computer from scratch and that your company's budget allows a very small amount of memory bandwidth. Which of the following characteristics would you choose in the ISA and the microarchitecture, and why? Explain briefly. [5 × 2 = 10 marks]
- Variable length instructions or fixed length instructions?
  - Complex instructions or simple instructions?
  - A large L2 cache or a small L2 cache? (L2 is the last-level cache)
  - An aggressive prefetcher or a conservative prefetcher?
  - Large cache blocks vs. small cache blocks?

[ 3.]

- (a) Consider the scenario given in table below, where "P" indicates a process and "R" indicated a resource.

Time	Action
1	P2 requests and is allocated R3
2	P4 requests and is allocated R4
3	P3 requests R4
4	P5 requests and is allocated R1
5	P1 requests and is allocated R2
6	P2 requests R2
7	P4 requests and is allocated R5
8	P1 requests R3
9	P3 requests R5
10	P4 releases R4, which is allocated to P3
11	P5 releases R1
12	P3 requests R3
13	P1 releases R2, which is allocated to P2
14	P4 releases R5, which is allocated to P3
15	P2 releases R3, which is allocated to P1
16	P2 releases R2

Use Holt's deadlocks modeling method to analyze the above scenario. [10 marks]

- (b) Is there a deadlock in the system above? Justify your answer. [05 marks]
- (c) Consider the situation given above in (a). Name the situations when the system was in critical condition and indicate what kind of action occurring next in the system? [05 marks]

[ 4.]

- (a) Throughput of a pipeline is inversely proportional to the bottleneck of the pipeline. Explain the statement. [05 marks]
- (b) An instruction execution path will take 9ns to execute an instruction in one-stage pipeline. However this logic path can be divided into any number of stages and the logic delay (9ns) can be subdivided equally as well. Moreover the sum of setup time of a latch and clock skew will be 1ns. Let  $s$  as the number of stages. Assume that the pipeline receives a set of instructions without branching instructions.
- What is the clock period  $T_{clock}$  in terms of  $s$ ? [05 marks]
  - What is the execution time of 101 instructions? [05 marks]
  - Calculate the optimum number of stages that the pipeline should have for minimum execution time of 101 instructions. [05 marks]

[ 5.] A magnetic disk system has the following parameters:

$T_s$  = average time to position the magnetic head over a track

$R$  = rotation speed of disk in revolutions per second

$N_t$  = number of bits per track

$N_s$  = number of bits per sector

- (a) Define the terms seek time and rotational delay. [02 marks]
- (b) Calculate the average time  $T_a$  that it will take to read one sector. [05 marks]
- (c) What is the transfer rate of an eight-track magnetic tape whose speed is 120 centimeters per second and whose density is 1600 bits per centimeter? [05 marks]
- (d) Specification of a hard disk of 1.2 GB made up with several platters is given as follows: 620 cylinders, 64 heads, and 63 sectors. The performance measuring utility shows the average seek time as 9ms. Disk rotational speed is calculated as 7200 rpm.
- (i) Calculate the average rotational delay. [03 marks]
- (ii) Calculate the number of bytes in a sector of the hard disk. (Note: bytes in a sector should be the nearest to the power of two value) [05 marks]

[ 6.]

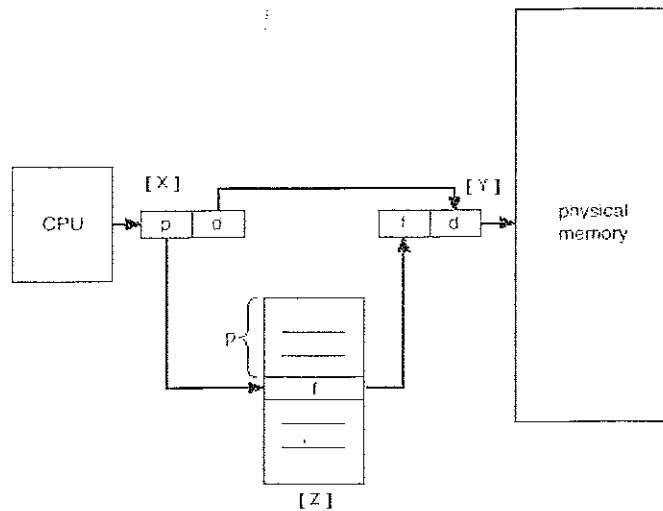
- (a) What are the levels in a File Management System between Basic File System and the Device? [04 marks]
- (b) Explain how non-contiguous (records) storage allocation method differs from the unblocked, variable-length records storage allocation method. [06 marks]
- (c) Draw a flowchart to implement reading and writing to the directory of non-contiguous storage allocation method with linking at the directory level. State all your assumptions. [10 marks]

[ 7.] Your job is to evaluate the potential performance of two processors, each implementing a different ISA. The evaluation is based on its performance on a particular benchmark. On the processor implementing ISA A, the best compiled code for this benchmark performs at the rate of 10 IPC. That processor has a 500 MHz clock. On the processor implementing ISA B, the best compiled code for this benchmark performs at the rate of 2 IPC. That processor has a 600 MHz clock.

- (a) What is the performance in MIPS (millions of instruction per second) of the processor implementing ISA A? [04 marks]
- (b) What is the performance in MIPS (millions of instruction per second) of the processor implementing ISA B? [04 marks]
- (c) Which is the higher performance processor? Explain. [06 marks]
- (d) Which is better? More RAM or a faster processor? Point out the reasons to support your answer. Answer should be in point form. [06 marks]

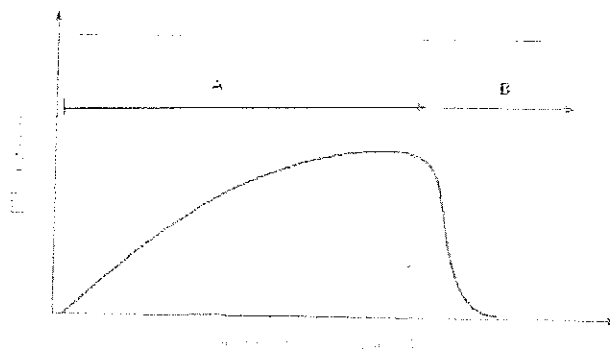
[ 8.]

- (a) Briefly explain the steps involved in handling a page fault. [04 marks]
- (b) Memory paging is a feature that permits extending the address space far beyond the available memory. [X] and [Y] denotes different addresses. Name the components given as [X], [Y] and [Z] in the following diagram (*Figure 1*) and describe how the extension of the address space happens. [06 marks]



*Figure 1: Memory Paging*

- (c) Page size is one of the parameters of a virtual memory. State one advantage and one disadvantage of choosing a large page size rather than a small one. [04 marks]
- (d) The following diagram (*Figure 2*) depicts CPU utilization vs degree of multiprogramming. Focus on the regions shown by (A) and (B) and describe the reasons for such a behavior. [06 marks]



*Figure 2: CPU Utilization vs Degree of multiprogramming*



