The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

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Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX3351 Electronics I**
Academic Year	: 2020/2021
Date	: 23rd January 2022
Time	: 0930-1230hrs
Duration	**: 3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Five (5)** questions in **Four (4)** pages.
3. Answer **All** the questions.
4. Answer for each question should commence from a new page.
5. Relevant charts / codes are provided.
6. This is a Closed Book Test **(CBT).**
7. Answers should be in clear hand writing.
8. Do not use red colour pens.

Q1. (a) Considering the behavior of the P-N junction in reverse and forward biased Modes, derive the characteristic curve of a practical diode. **(4 Marks)**

(b) Consider the current-limiting series regulator circuit in Figure-Q1 where Z is a Zenner diode with a breakdown voltage of 6V and T1 and T2 are identical Si transistors with a base-emitter voltage drops of 0.7V in each. $R_L = 20\Omega$. Further assume the operational amplifier to be ideal and the minimum current through the Zenner to maintain the breakdown is 20mA. The regulator is fed with an input supply V_{in} varying in the range $20V - 30V$.

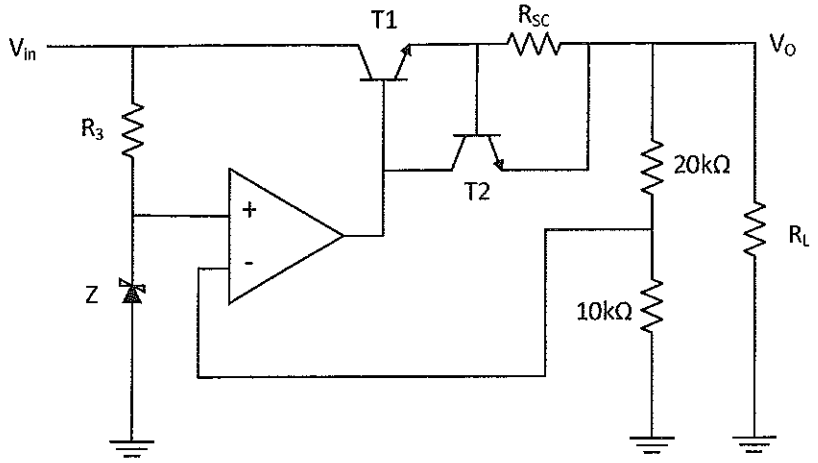

Figure-Q1

i. Calculate a suitable value for R_3 to maintain the Zenner at breakdown. **(4 marks)**

ii. Explain the operation of the circuit when the input voltage increases from 20V to 30V. **(4 marks)**

iii. Calculate the regulated output voltage V_o. **(4 marks)**

iv. Calculate the value of R_{SC} to limit the maximum load current to 0.5A. **(4 marks)**

Q2. Figure-Q2 shows a transistor amplifier circuit arrangement. Here T is a Silicone transistor having $\beta = 80$.

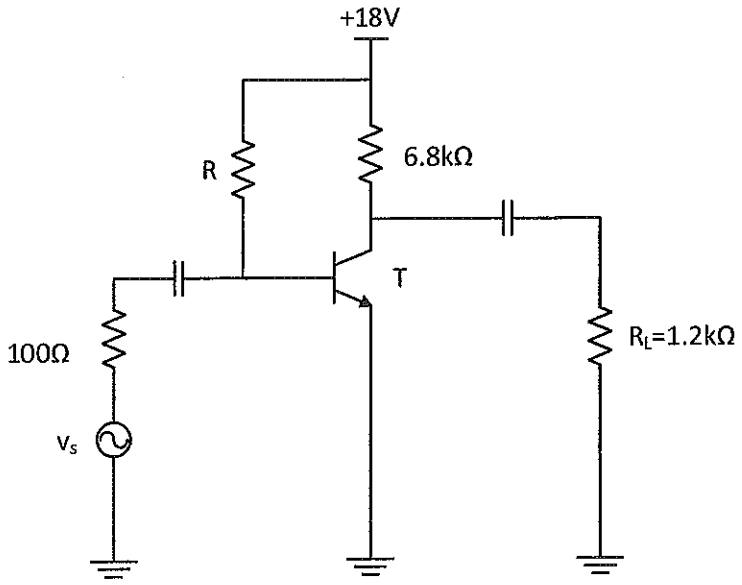

Figure-Q2

(a) What is the bias configuration of the amplifier? **(1 Mark)**

(b) Find expressions for the collector current and the voltage across collector-emitter terminals (V_{CE}) in terms of R. **(4 Mark)**

(c) Draw the DC load line for the above amplifier and mark the Q point. **(4 Mark)**

(d) Hence, find a suitable value for resistor R to produce a maximum peak-to-peak output swing without distortion. **(6 Mark)**

(e) What is the maximum possible distortion-free peak-to-peak value of the supply voltage v_s when R is set to the value calculated in (d)? **(5 Mark)**

Q3. A small signal circuit is shown in Figure-Q3. Let, $V_{CC} = 18V$, $R_1 = 100k\Omega$, $R_2 = 56k\Omega$, $R_E = 1k\Omega$, $r_s = 1k\Omega$ and $R_L = 50\Omega$. The transistor has the following h parameter values.

$h_{fc} = -101, h_{rc} = 1$ and $h_{ic} = 1.4k\Omega$. h_{oc} is negligibly small.

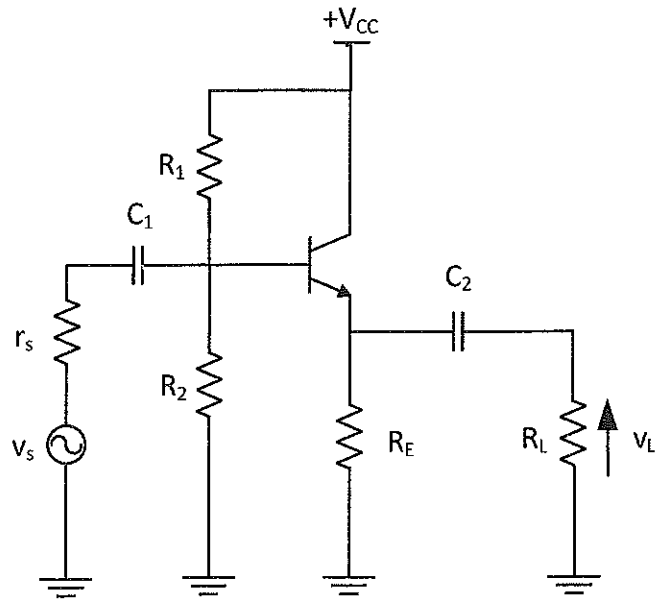

Figure-Q3

(a) Draw the AC h parameter equivalent circuit for the amplifier in Figure-Q3. **(5 Marks)**

(b) Using above parameter values, find the following.

i. Current gain **(3 marks)**
ii. Voltage gain **(3 marks)**
iii. Power gain **(3 marks)**
iv. Input impedance **(3 marks)**
v. Output impedance **(3 marks)**

Q4.

(a) List and explain three characteristics of an ideal operational amplifier. Discuss the deviations in practical operational amplifiers. **(3x2 Marks)**

(b) An inverting Schmitt trigger circuit is shown in Figure-Q4.

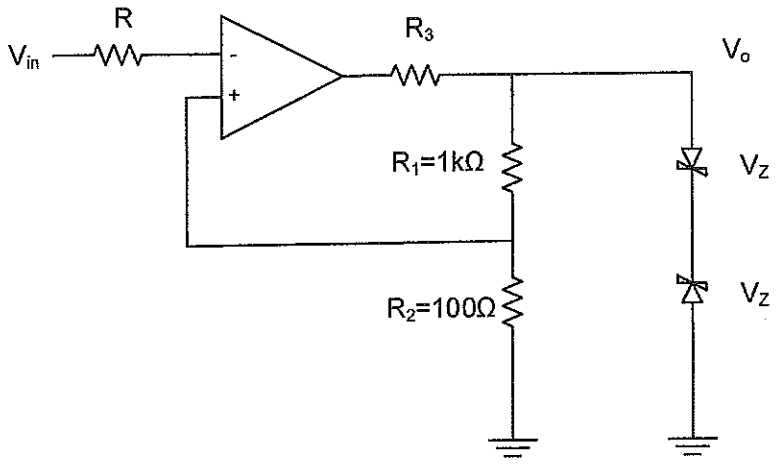

Figure-Q4

Assume that both Zenner diodes are identical and the Zenner voltage and the forward barrier voltage are 6.3V and 0.7V respectively.

i) Draw the transfer characteristics. **(4Marks)**
ii) Explain the hysteresis observed in transfer characteristics. **(4Marks)**
iii) Draw the output waveform for an input of $v_{in} = 2\sin(10\pi t)$. **(6Marks)**

Q5.

(a) Perform the calculation 22-31 in 8 bit 2's complement arithmetic. **(4 Marks)**

(b) Carry look-ahead adder is a concept used in modern microprocessor ALUs to generate all carry bits required in adding two multi-bit numbers using a combinational circuit. This eliminates the need for long waiting in order to receive the rippled carry bits. Let $A = a_4a_3a_2a_1$ and $B = b_4b_3b_2b_1$ are two 4 bit numbers for addition. Consider the addition of a single bit position with a full adder.

i. Show that the Boolean expression for the carry at the n-th bit ($n = \{1,2,3,4\}$) can be expressed in the form $C_n = G_n + C_{n-1}P_n$ where G_n and P_n are Boolean functions of $a_n$and b_n.
[You should clearly show the steps including the truth table and minimization] **(6Marks)**

ii. Hence show that C_n can be expressed interms of c_1, a_n and b_n only ($n = \{1,2,3,4\}$). **(4Marks)**

iii. Implement the complete carry generation combinational logic circuit using only NOR gates. **(6Marks)**