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The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Bachelor of Technology Honors in Engineering – Level 6
ECX 6151 – DIGITAL ELECTRONIC SYSTEMS

FINAL EXAM 2015/2016

Date: 26-11-2016 **Time:9.30AM -12:30 noon**
Time Allowed: 03 hours

INSTRUCTIONS TO CANDIDATES

1. This question paper contains two parts in **SECTION A** and four questions in **SECTION B** on two pages.
2. Answer **ALL PARTS** in **SECTION A.** [70 marks]
3. Answer any **TWO (2)** questions from **SECTION B.** [30 marks]
4. Refer the Annexure of the VHDL syntax given in page three to write VHDL code.
5. Clearly state your assumptions if any.

SECTION A: Answer ALL questions [70 marks]

Question 1

(a) Design a control of a vending machine for the following specifications.

Design Specifications

- The vending machine accepts only Rs 10 coins.
- The machine can dispense the following items
  - water (W)- Rs 30.00
  - milk (M) – Rs40.00
  - yoghurt drink (Y) – Rs 60.00
- The machine has a coin return (CR) button.
- Only one input is active at a time.
- A product can be dispensed in one clock cycle.
- If more than Rs 60.00 is inserted the money is returned.
- If no input is active, the state machine stays in the current state.
- The outputs of the vending machine are,
  - Coin return (CRO)
  - Water out (WO)
  - Milk out (MO)
  - Yoghurt drink out (YO)
  - Ten rupee coins out (TO)

(i) Compute the state diagrams for both Mealy and Moore and compare the two designs. [20 marks]

(ii) Compute the state transition table for the minimal design identified in Q1(a)(i). [10 marks]

(iii) Write the behavioural VHDL code for the minimal design identified in Q1(a)(i). [30 marks]

PART(b)

1. Explain the term propagation delay of a gate. [02 marks]
2. State the three types of delay models available in VHDL to specify the delays in gates, interconnections and very small delays associated with a circuit. [02 marks]
3. Describe the term testability of a VLSI circuit. [02 marks]
4. Identify all possible (a) fault sites and (b) single stuck-at faults in a two input NAND gate. [02 marks]
5. Explain the term path sensitization. [02 marks]

SECTION B: Answer any TWO questions [30 marks]

Question 2 [15 marks]

Construct a block diagram and ASM chart for a digital system which counts a remote control car going in each direction. Two sensors, L-sensor and R-sensor, are placed side by side. The corresponding signal transition from 0 to 1 indicates when the car goes past. When the car is going left, it will first cause an L signal, then an R signal, while a bike going right will cause a R signal followed by an L signal. If the first signal isn't followed by the expected second signal then it should return to the reset state. The datapath consists of two counters for each direction and it receive a count signal generated by the digital system you designed. Assume that only one remote control car will ride at a time.

Question 3 [15 marks]

Construct a Moore model finite state machine to detect the "1011" sequence and write the designed using behavioral VHDL. Your design should detect overlapping sequences.

Question 4 [15 marks]

Construct a counter that counts the numbers in sequence 000 -> 010 -> 011 ->111 and returns to 000. Draw the state diagram, the excitation table and the design using J-K flip flops.

Question 5 [15 marks]

Design a counter which cycles through the binary sequence (1,2,4,5,6,7) using J-K flipflops. Show that when states 000 and 011 are used as don't care statements the counter may not operate properly. Suggest how to correct this problem.

Annexure

Syntax of selected instructions of the VHDL

```
ARCHITECTURE architecture_name OF entity_name IS
  [declaration part]
BEGIN
  Concurrent statements part
END architecture_name
```

```
CASE expression IS
  WHEN value=> statements;
  WHEN value=> statements;
  WHEN OTHERS statements;
END CASE;
```

```
COMPONENT component_name
  PORT (port1_name : port1_type;
        port2_name : port2_type;
        ...);
END COMPONENT [component_name];
```

```
ENTITY entity_name IS
  PORT (port1 : port1_type;
        port2 : port2_type;
        ...);
END entity_name;
```

```
IF condition THEN
  Sequence of statements
  {ELSIF condition THEN
     Sequence of statements}
[ELSE
  Sequence of statements]
END IF;
```

```
LIBRARY library_name;
```

```
Instance_label: component_name PORT MAP (first_port, second_port,
                                         third_port, ...);
Instance_label: component_name PORT MAP (formal1=> actual1,
                                         formal1=> actual1,
                                         formal1=> actual1, ...);
```

```
[process_label:] PROCESS (signal1, signal2, ...)
                   [declaration part]
                 BEGIN
                   Sequential statements part
                 END PROCESS;
```

```
SIGNAL signal_name : signal_type;
```

```
TYPE type_name;
```

```
USE library_name.type_expression.inclussion;
```

```
WAIT FOR time_expression;
WAIT ON signal1, signal2, ...;
WAIT UNTIL condition;
```

```
WHILE condition LOOP
  Sequential statements
END LOOP;
```