THE OPEN UNIVERSITY OF SRI LANKA

DEPARTMENT COMPUTER SCIENCE

B. SC. DEGREE PROGRAMME 2021/2022

FINAL EXAMINATION

CSU5306: DIGITAL ELECTRONICS

DURATION: TWO HOURS (2 HOURS)

Date: 01.11.2022 **Time: 1.30 pm – 3.30 pm**

Answer **FOUR** Questions **ONLY.** All questions carry equal marks.

Q1.

A food manufacturing plant which is making grain burger patties is using an automated plant for manufacturing. Now they require an alert system to ensure smooth operation of the plant.

The plant consists of three Units: **Storage, Process, and Package.** In the Storage section, the raw grain is stored in storage tanks. 5 varieties of grain are used for the grain patties. Each of these tanks requires certain conditions: Temperature must be below 30 degrees of Celsius and humidity must be below 13%. Each morning at 8.00 am raw grain is released into a Soaking tank in the Process unit before releasing grain. Each storage tank must at least be 75% full and 25% of the tanks will be used in each batch of grain patties.

The Soaking tank will soak the grain in water for about 3 hours. Then the soaked grain will be transported through a conveyor belt to a crusher in 5kg blocks. The crusher takes 2 minutes to make a grain paste. Hence the conveyor belt speed must be at 2m/ minute. Then the grain paste will be conveyed to a mixing bowl and additional ingredients and seasoning will be added manually. The mixer will run at a speed of 15rpm, and the mixed grain paste will be fed into a molding machine via a conveyer. Then the grain mixer will be made into grain patties and the same conveyor passes the patties through a cooling unit at 2 degrees of Celsius. The cooled grain patties are sent to the Package unit via the same conveyer belt. 6 patties will be packed into one box and 6 boxes are packed into a platter automatically. Then the platters will be stored in the package unit under 4 degrees Celsius for delivery.

Use the paragraph to answer the questions below.

(i) Derive a Truth table for the operation of the Storage Unit. Using K'Map simplification method derive the simplified Boolean equation for storage unit function

(ii) What are the conditions that must be satisfied in the Process unit?

(iii) With the parameters identified in section (ii) develop a Boolean equation for successful grain patties making. (Use Min-terms) Minimize the Boolean equation using Boolean Algebra rules. Mention the rules used.

(iv) Draw separate logic circuits for the storage unit function and process unit function.

(v) Combine the two circuits in (iv) to present the full operation of the manufacturing plant. (Use any combinational circuits for the data management)

Q2.

(i) Identify the Circuit and derive the Truth Table for the outputs of the circuit presented in Figure 1. (The ICs used in the diagram are 74HC04, 74HC11, 74HC11 from the left.)

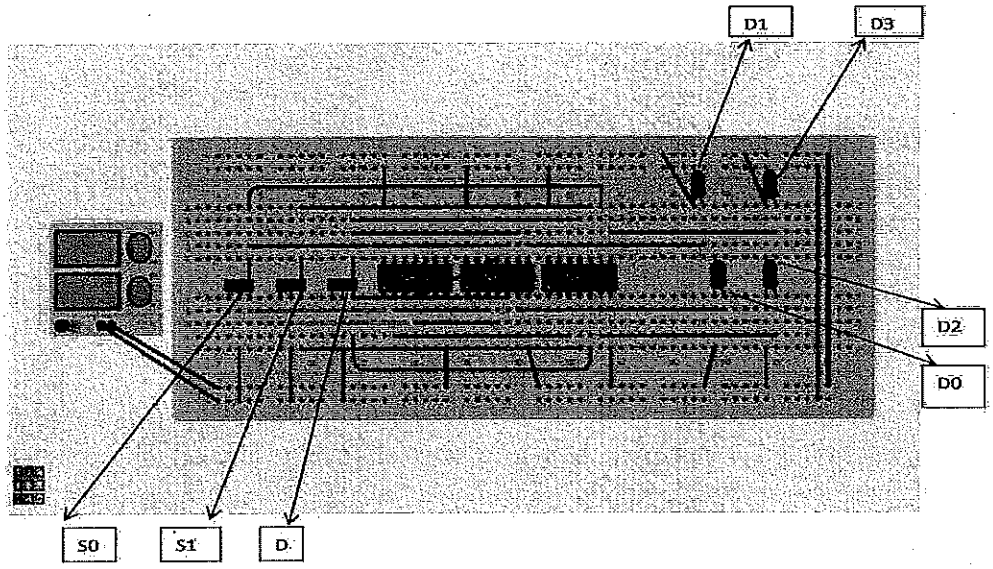
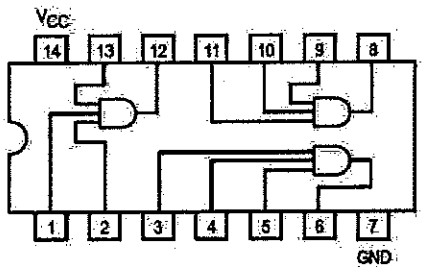
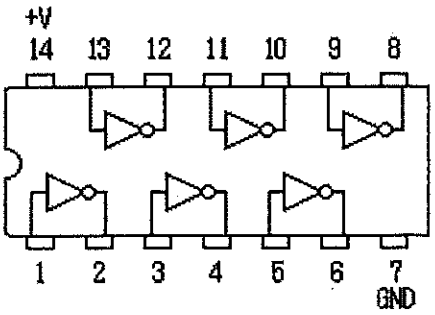


Figure 1: Circuit for the Question 3 section i

Data Sheet for ICs



74HC11



74HC04

(ii) Draw the logic diagram of the 4-bit Full Adder.

(iii) Derive the truth table for 4-bit Full Subtractor Circuit.

(iv) Explain the two forms of multiplexers?

(v) Draw the logic symbol for the decimal to BCD encoder.

(vi) Using the 2-1 multiplexer, develop a 16-1 Multiplexer.

Q3.

(i) State the following features for the Binary, Octal, Decimal and Hexadecimal number systems.

a. Range of Values

b. Digits

c. Maximum and Minimum value

(ii) Convert the following Decimal numbers into Binary, Octal and Hexadecimal. Clearly show the steps.

a. 126

b. -234

(iii) Solve the following sums using BCD addition.

a. 0010 0111 + 0001 1000

b. 1000 0110 + 0001 0011

(iv) Describe the Alphanumeric Code with its contents.

(v) Briefly describe the evolution of Alphanumeric Codes.

Q4.

(i) What are the classes of Sequential Logic circuits?

(ii) Explain the function of the Clocked SR flip flop. Use Logic circuit, Truth table and Timing diagram as needed.

(iii) Explain the Preset and Clear signals and identify the difference from the Direct Set and Direct Clear signals.

(iv) Derive the Asynchronous sequential circuit for the circuit described by the state table. Clearly show the steps.

Present State		Next State			
		X = 0		X = 1	
0	0	0	0	0	1
0	1	0	1	1	1
1	0	1 ′	0	0	0
1	1	1	0	1	1

(v) Discuss the stability of the above circuit (in iv).

Q5.

(i) Draw the IC diagram for the Four Position Binary Counter using TTL JK flip flop.

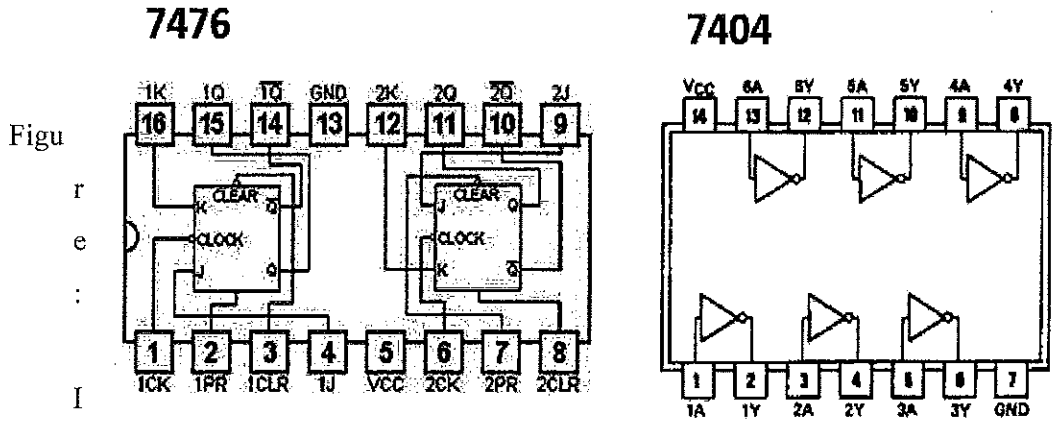


Figure: IC s for the Q5 section i

(ii) How does an Asynchronous Counter with a truncated sequence used as frequency divider? Explain with an example.

(iii) Draw a Timing Diagram for a 4-bit Serial-In to Parallel-Out Shift register.

(iv) Compare 4-bit Synchronous Ring Counter vs. 4-bit Johnson Ring Counter.

(v) Draw a block diagram for the Synchronous counter which can count upto 13.

Q6.

(i) Briefly explain the components of the CPU that are used in the Fetch Execute cycle.

(ii) Explain the "data write" and "data read" function of a 1-bit memory cell made with a D flip flop.

(iii) Describe the following interaction policies.

a. No Read Through

b. Write Through with Write Allocate

c. Write Back with No Write Allocate

(iv) What is the importance of Digital memory for the computer?

(v) Implement the logic circuit of the PLA for the following Boolean functions.

F1 = AB' + A'C + ABC'

F2 = (A'C + BC)'

*****End of Examination Paper *****