THE OPEN UNIVERSITY OF SRI LANKA
BACHELOR OF TECHNOLOGY - LEVEL 5
ECX5236 – COMPUTER ARCHITECTURE
FINAL EXAMINATION 2015

DURATION: THREE HOURS

DATE: 01st December 2016 **TIME: 09:30 – 12:30 HOURS**

Answer any ***five*** questions. All questions carry equal marks.

1.

(i) Distinguish MIMD multiprocessors from multi-computers or computer networks.

(ii) What are the salient features of RISC architecture and CISC architecture? Provide advantages and disadvantages of each architecture.

(iii) What are the advantages and disadvantages of a Superscalar implementation and a VLIW approach?

(iv) A processor executes 10 million floating point and one million overhead instructions in 50 ms. What is the MFLOPS rating of this processor? What would be the MIPS rating of the same processor?

2.

(i) Draw typical virtual machine schematics for different styles of Instruction Set Architecture (ISA) i.e. Accumulator, Memory-Memory, Stack, Load-Store.

(ii) Describe advantages and disadvantages of each virtual machine in question 2. (I) comparing each other.

(iii) In a source code a programmer declared an array of integers. All elements of the array are signed 16-bit integers. Later the programmer declared another array of floating point numbers at the same starting pointer of the integer array. Assume all the floating pointer number elements are in the following format and values are saved in the integer array.

S (1 bit)	Exponent (7-bit)	Mantissa (24-bit)

(a) Draw a diagram to show how these two arrays are stored in the memory. Assume that the memory is byte addressable.

(b) Explain when you get positive numbers in the floating point array.

(c) In order to get values greater than 1 in all elements of the floating point array which numbers do you have to save in the integer array.

(d) What will be decimal values of the elements of the floating point array if you save the following values in the integer array in the given order: 1408, 00, -96 and -32768 in decimal.

3.

(i) What are the advantages of Synchronous communication and Asynchronous communication?

(ii) Briefly describe the following I/O control systems: Programmed I/O, Interrupt I/O, and Coprocessor I/O.

(iii) What is the basic advantage of interrupt initiated data transfer over the transfer under program control without an interrupt?

(iv) Consider a processor with programmed I/O that executes instructions at a rate of 0.1 MIPS. An I/O subroutine for writing to floppy disk requires 10,000 instructions and the disk has a total latency of 100ms. What is the suspend time of the main program?

4. You need to control a device through a computer. This device receives a four-bit command either serially or parallel and executes it. After its execution, the device gives a signal to the computer to indicate that it can receive the next command.

(i) Draw a block diagram to show how you are going to connect the device to a computer using a COM port. You need to indicate the connections through necessary 8250 Family Registers of a serial port and give a brief description of your setup and working procedure. For necessary port register description refers the appendix.

(ii) Give a flowchart of a subroutine that controls the device, and clearly state all values of port registers and their addresses wherever they are used. For necessary port register description refers the appendix.

(iii) How do you set up a connection for the same purpose through a parallel port of a computer? You need to indicate the connections through a parallel port and give a brief description of your setup and working procedure. For necessary port register description refers the appendix.

(iv) Give a flowchart of a subroutine that controls the device using the parallel port. Clearly state all values of port registers and their addresses wherever they are used. For necessary port register description refers the appendix

5. The Fig. 1 shows a linear pipeline with k stages (S_i) separated by latches (L). Common clock (C) is applied to all latches simultaneously. Each stage S_i has a time delay τ_i, where $i=1,2,...,k$.

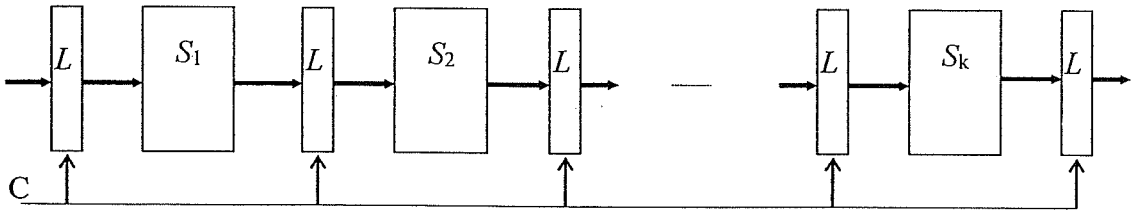


Fig. 1 Linear pipeline with k stages.

(i) If the time delay of the each latch is τ_l what is the clock period (τ) of the pipeline?

(ii) Derive an equation to calculate the speedup (s) of the k stage linear pipeline over an equivalent nonpipeline processor.

(iii) Show that maximum achievable speedup of a linear pipeline is equal to its number of stages.

(iv) Calculate the maximum speedup of a linear pipeline with 4 stages, where $\tau_1 = \tau_3 = 40$ ns, $\tau_2 = 80$ ns, $\tau_4 = 50$ ns and $\tau_l = 10$ ns.

(v) Explain why the speedup you get in (5.iv) is less than 4. How can you improve the speedup in this case?

6.

(i) Name three organizations of cache memory and describe them briefly.

(ii) Comment on the following statement giving reasons.

"Hit ratio can be improved by using faster memory, i.e. memory with less access time."

(iii) Why are the first level caches usually split (instructions and data are in different caches) while the L2 is usually unified (instructions and data are both in the same cache)?

(iv) For a data cache with a 92% hit rate and a 2-cycle hit latency, calculates the average memory access latency. Assume that latency to memory and the cache miss penalty together is 124 cycles. Note: The cache must be accessed after memory returns the data.

7.

(i) Explain the Amdahl's law and derive an equation for that.

(ii) The MIPS rating of a processor is 1000. However the processor requires at least two memory access per instruction. The memory latency of the system is 10 ns.

(a) What is the MIPS rating of the system.

(b) The performance of the system depends very much on the memory. Propose three solutions for this performance problem. Describe them briefly.

(c) If you are able to double the MIPS rating of the processor what is the achievable overall speedup of the system. Assume that there is no change in memory latency. Solve the problem using the Amdahl's law.

8.

(i) Briefly describe the disk allocation schemes, Contiguous Allocation and Linked Allocation.

(ii) Briefly describe the RAID levels. What is/are the suitable RAID level/s for the following systems/situations?

(a) Data-critical real-time systems

(b) Transferring large quantities of non-critical data

(c) Data critical systems with high data transfer rates

(iii) A disk drive has eight surfaces, with 512 tracks per surface and a constant 64 sectors per track. Sector size is 1 Kbytes. The average seek time is 8ms, the track-to-track access time is 1.5ms, and the drive runs at 3600 rpm. Successive tracks in a cylinder can be read without head movement.

(a) What is the drive capacity?

(b) What is the average access time for the drive?

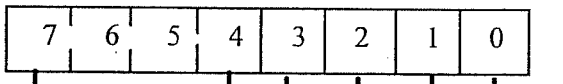
Appendix

8250 Family Register Definitions

Register Name	Offset	Abbreviation	Access Type
Receiver Buffer Register	0	RBR	Read Only
Transmit Holding Register	0	THR	Write Only
Interrupt Enable Register	1	IER	Read/Write
Interrupt Identification Register	2	IIR	Read Only
FIFO Control Register (16550)	2	FCR	Write Only
Line Control Register	3	LCR	Read/Write
Modem Control Register	4	MCR	Read/Write
Line Status Register	5	LSR	Read Only
Modem Status Register	6	MSR	Read Only
Divisor Latch (16 bits)	0/1	DL	Read/Write

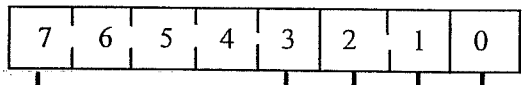
Base address of COM1 - 3F8h Base address of COM2 - 2F8h

IER



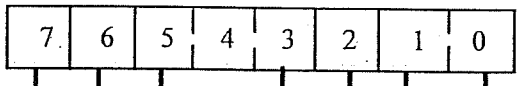
1- Received Data Available
1- Transmit Holding Register Empty
1 - Line Status
1 - Modem status (CTS, DSR, DCD or RI changes state)
Not used (= 0)

IIR



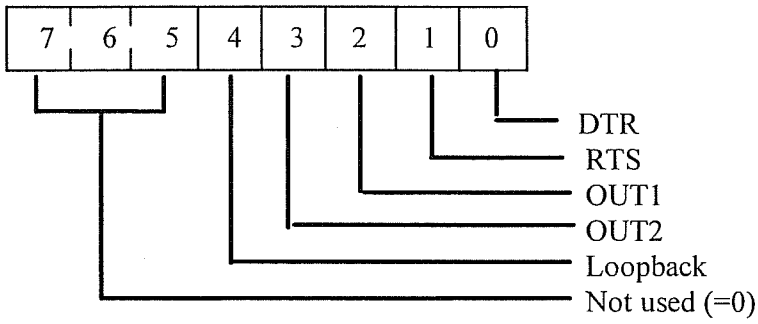
1 - No interrupt Rending
00 - Modem Status Interrupt
01 - Transmit Holding Register Empty
10 - Received Data Available
11 - Line Status
Not used (= 0)

LCR

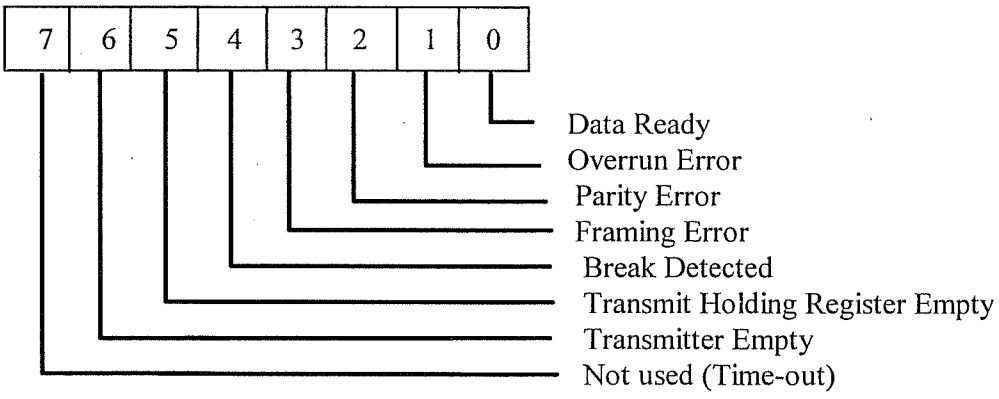


Word length Select
00 - 5 bits 10 - 7 bits
01 - 6 bits 11 - 8 bits
Number of Stop Bits
0 - 1 bit 1 - 2 bits
Control Bits
000 - No parity 100 - No Parity
001 - Odd Parity 101 - Mark Parity
010 - No Parity 110 - No Parity
011 - Even Parity 111 - Space Parity
Break Control
Divisor Latch Access Bit
1- Divisor Latch
0 - as usual RBR/ THR and IER

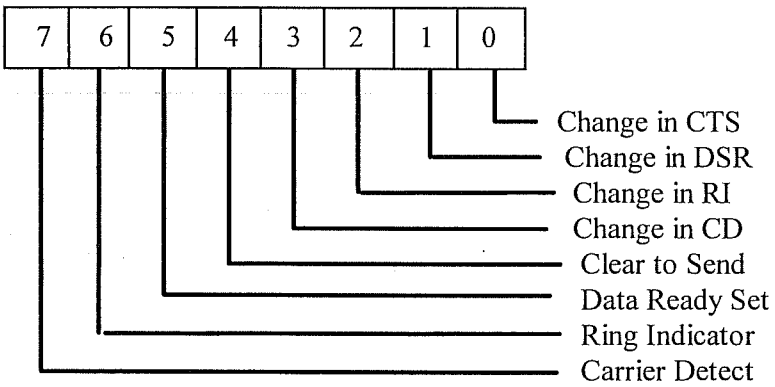
MCR


7
6
5
4
3
2
1
0
DTR
RTS
OUT1
OUT2
Loopback
Not used (=0)

LSR


7
6
5
4
3
2
1
0
Data Ready
Overrun Error
Parity Error
Framing Error
Break Detected
Transmit Holding Register Empty
Transmitter Empty
Not used (Time-out)

MSR


7
6
5
4
3
2
1
0
Change in CTS
Change in DSR
Change in RI
Change in CD
Clear to Send
Data Ready Set
Ring Indicator
Carrier Detect

Appendix A

Parallel port connector description

Pin: D-sub	Signal	Function	Source	Register		Inverted at con-nector?	Pin: Centron-ics
				Name	Bit #		
1	nStrobe	Strobe D0-D7	PC[1]	Control	0	Y	1
2	D0	Data Bit 0	PC[2]	Data	0	N	2
3	D1	Data Bit 1	PC[2]	Data	1	N	3
4	D2	Data Bit 2	PC[2]	Data	2	N	4
5	D3	Data Bit 3	PC[2]	Data	3	N	5
6	D4	Data Bit 4	PC[2]	Data	4	N	6
7	D5	Data Bit 5	PC[2]	Data	5	N	7
8	D6	Data Bit 6	PC[2]	Data	6	N	8
9	D7	Data Bit 7	PC[2]	Data	7	N	9
10	nAck	Acknowledge (may trigger interrupt)	Printer	Status	6	N	10
11	Busy	Printer busy	Printer	Status	7	Y	11
12	PaperEnd	Paper end, empty (out of paper)	Printer	Status	5	N	12
13	Select	Printer selected (on line)	Printer	Status	4	N	13
14	nAutoLF	Generate automatic line feeds after carriage returns	PC[1]	Control	1	Y	14
15	nError (nFault)	Error	Printer	Status	3	N	32
16	nInit	Initialize printer (Reset)	PC[1]	Control	2	N	31
17	nSelectIn	Select printer (Place on line)	PC[1]	Control	3	Y	36
18	Gnd	Ground return for nStrobe, D0					19,20
19	Gnd	Ground return for D1, D2					21,22
20	Gnd	Ground return for D3, D4					23,24
21	Gnd	Ground return for D5, D6					25,26
22	Gnd	Ground return for D7, nAck					27,28
23	Gnd	Ground return for nSelectIn					33
24	Gnd	Ground return for Busy					29
25	Gnd	Ground return for nInit					30
	Chassis	Chassis ground					17
	NC	No connection					15,18,34
	NC	Signal ground					16
	NC	+5V	Printer				35

[1]Setting this bit high allows it to be used as an input (SPP only)

[2]Some Data ports are bidirectional.

Parallel port register definitions

Base address: 0378h

Data Register (Base Address)					
Bit	***Pin: D-sub***	**Signal Name**	**Source**	**Inverted at connector?**	**Pin: Centronics**
0	2	Data bit 0	PC	no	2
1	3	Data bit 1	PC	no	3
2	4	Data bit 2	PC	no	4
3	5	Data bit 3	PC	no	5
4	6	Data bit 4	PC	no	6
5	7	Data bit 5	PC	no	7
6	8	Data bit 6	PC	no	8
7	9	Data bit 7	PC	no	9
Some Data ports are bidirectional. (See Control register, bit 5 below.)					
Status Register (Base Address +1)					
Bit	***Pin: D-sub***	**Signal Name**	**Source**	**Inverted at connector?**	**Pin: Centronics**
3	15	nError (nFault)	Peripheral	no	32
4	13	Select	Peripheral	no	13
5	12	PaperEnd	Peripheral	no	12
6	10	nAck	Peripheral	no	10
7	11	Busy	Peripheral	yes	11
Additional bits not available at the connector: 0: may indicate timeout (1=timeout). 1, 2: unused					
Control Register (Base Address +2)					
Bit	***Pin: D-sub***	**Signal Name**	**Source**	**Inverted at connector?**	**Pin: Centronics**
0	1	nStrobe	PC[1]	yes	1
1	14	nAutoLF	PC[1]	yes	14
2	16	nInit	PC[1]	no	31
3	17	nSelectIn	PC[1]	yes	36
[1]When high, PC can read external input (SPP only). Additional bits not available at the connector: 4: Interrupt enable. 1=IRQs pass from *nAck* to system's interrupt controller. 0=IRQs do not pass to interrupt controller. 5: Direction control for bidirectional Data ports. 0=outputs enabled. 1=outputs disabled; Data port can read external logic voltages. 6,7: unused					