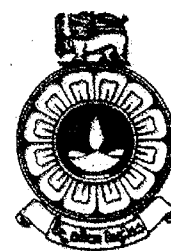THE OPEN UNIVERSITY OF SRI LANKA

DEPARTMENT COMPUTER SCIENCE

B. SC. DEGREE PROGRAMME 2023/2024

FINAL EXAMINATION

CSU5306: DIGITAL ELECTRONICS

DURATION: TWO HOURS (2 HOURS)

Date: 25.10.2023	Time: 1.30 pm – 3.30 pm

General Instructions

1. Read all instructions carefully before answering the questions.

2. This question paper consists of **06** questions on **04 pages**.

3. Answer any **04** questions only. All questions carry equal marks.

4. The answer for each question should commence from a new page.

5. Draw fully labeled diagrams where necessary

6. Involvement in any activity that is considered an exam offense will lead to punishment

7. Use blue or black ink to answer the questions.

8. Clearly state your index number in your answer script

Q1.

   i.   Convert the following binary (base 2) numbers into decimal. Clearly show the steps.

        a. 110111

        b. 100111

  ii.   Convert the following decimal numbers into binary. Clearly show the steps.

        a. 56

        b. 94.625

  iii.   Discuss the importance of Binary Representation for the Digital Computer.

  iv.   Prove the following Boolean Algebra Rules. Clearly show the steps.

        a. Distributive Law

        b. De Morgan's Theorem

Q2.

    i.   Simplify the following Truth Table using Minterm Canonical form. (you can use any simplification model)

A	B	C	Q
0	0	0	0
0	1	0	1
0	0	1	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

    ii.   Draw the simplified logic circuit.

    iii.   Redraw the circuit in (ii) using any universal logic gate.

   iv.   Briefly describe the evolution of Alphanumeric Codes.

Q3.

    i.   Briefly describe the functions of Combinational Logic circuits in ALU.

    ii.   Draw a 4-bit Adder circuit with the help of the schematic diagram for the one-bit adder circuit.

    iii.   Draw the logic diagram of the Binary Decoder for 1101(in base 2)

    iv.   Draw the logic circuit of the 4-1 Multiplexer.

Q4.

    i.   Explain the reasons for considering SR flip flop as only a theoretical Flip Flop.

    ii.   Explain how to derive a D-Flip Flop using an SR flipflop.

iii. Draw the IC circuit for the Master-Slave JK flip flop (74HC76)

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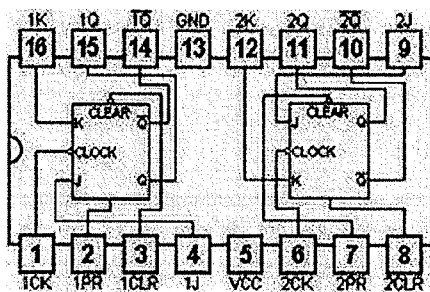
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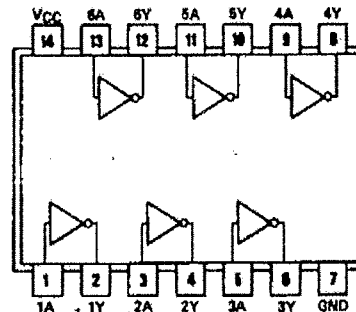
iv. Derive the asynchronous sequential circuit for the circuit described by the following State Table. Clearly show the steps.

Present State		Next State			
		X = 0		X = 1	
0	0	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	1	1	1	1	0

Q5.

i. Discuss the uses of Shift Registers in digital computers.

ii. Edge-triggered JK flip flops can be used for counters. Explain the counting function of an array of 4-bit JK flip flops using a timing diagram.

iii. Design a truncated counter circuit to count to 1001b.

iv. Explain how a divide-by-n counter can be used as a frequency divider. Use TTL 7493 IC as an example to describe the function.
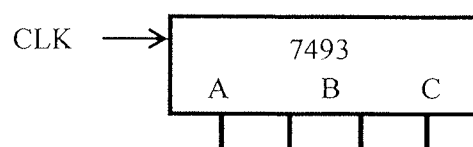
Q6.

   i.   Briefly discuss about the Digital Memory.

  ii.   Describe the following interaction policies.

        a. No Read-Through

        b. Write Through with Write Allocate

        c. Write Back with No Write Allocate

 iii.   Derive a 16-bit RAM using a one-bit memory cell (Use properly labeled block Diagrams).

 iv.   What are the ways we can create Programming Logic Devices. Use diagrams to explain.

-End of Examination Paper –