The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX3336 Communications and Computer Technology**
Academic Year	: 2021/2022
Date	: 09th of February 2023
Time	: 0930 – 1230hrs
Duration	: **3 hours**

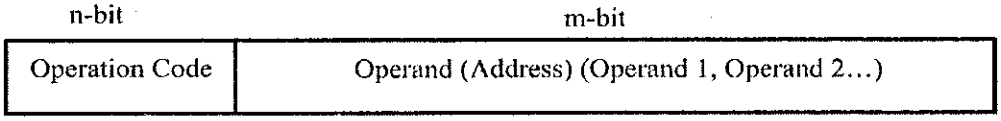
General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Four (4)** questions on **Five (5)** pages.
3. Answer all **four** questions.
5. Answer for each question should commence from a new page.
6. This is a Closed Book Test **(CBT).**
7. Answers should be in clear handwriting.
8. Do not use red colour pens.

Question 1

You can use the instruction set of the Accumulator Architecture given in Annexure 1 when answering the questions.

i.) The format for a simple instruction is given below.



A simple instruction format

a) Briefly explain what is stated as *opcode* and *operand.*

[02 Marks]

b) Define the instruction format using an example for each instruction type given below.

i. Zero-address instruction
ii. One address instruction

[02 Marks]

ii.) LOADacc #7 instruction is used to copy the operand to the Accumulator.

a) Draw a diagram and explain the instruction fetch and execution cycle for the instruction LOADacc #7, which is the first instruction of a program stored in the location 0100H. Briefly explain how the MAR, PC, MBR, CU and IR are involved during the operation.

[10 Marks]

b) Buses are used to send control signals, addresses and data between the processor and other components. Differentiate between the three types of buses used in a general-purpose computer system.

[06 Marks]

iii.) Draw appropriate diagrams and briefly explain the addressing modes of the instructions LOADacc #2, LOADacc 15, and LOADAcc @5

[06 Marks]

iv.) Write a program to find the smallest number of three values, *X1*, *X2* and *X3* and save the result in memory location 50H, where *X1*, *X2* and *X3* >*0*

X1=2, *X2* is given in memory locations 15H, and memory location 5 contains the address of the location where the target address *X3* is stored. Clearly state if you make any assumptions.

[10 Marks]

v.) If 50 and 60 are addresses of two memory locations, which of the following cannot be a valid instruction for an Accumulator based computer system? Briefly explain the rationale for selecting the answers.

a) LOADacc 50
b) PUSH 60
c) SUB 60
d) POP

[04 Marks]

Question 2

Write all relevant intermediate steps when answering questions from (i.) to (iv.)

i.) Convert the following decimal integer and fraction to binary.
   a) 87 **[01 Mark]**
   b) 0.320 (Truncate answer at 4th bit after binary point) **[02 Marks]**

ii.) Perform the following binary arithmetic operations;
   a) 1000110 + 1001110 (show the carry bits clearly) **[02 Marks]**
   b) 10101 * 1011 (show the partial products clearly) **[03 Marks]**

iii.)
   a) Calculate the decimal equivalent of the number -101011.01_2 **[01 Mark]**
   b) Represent the number in above a), in IEEE754 binary floating point single precision format. Show the steps clearly. **[03 Marks]**
   c) Calculate the value of y in the following equation.
   $21_8 - 100011_2 - 212_4 = -211_y$ **[03 Marks]**

iv.) Perform -8-17 using binary 2's complement techniques. **[05 Marks]**

Question 3

i.) Define the following terms associated with computer networks: **[06 Marks]**
   a) Protocol
   b) Error control
   c) Flow control

ii.) Compare and map the different layers of the OSI and the TCP/IP reference architectures. **[04 Marks]**

iii.) Describe the three modes of propagation of radio frequency wave signals:
   (i) ground wave propagation,
   (ii) tropospheric propagation, and
   (iii) direct wave propagation.
   Indicate the frequency bands and propagation impairments in each of the three propagation modes. **[06 Marks]**

iv.) Calculate the total gain (in dB) of the system shown in Figure1 where Pin = 10mW, P1 = 5mW, P2 = 4mW, P3 = 2mW and P4 = 1mW. **[04 Marks]**

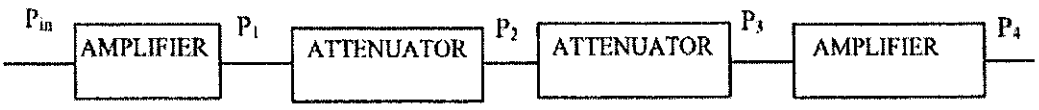


Figure 1

Question 4

i.) Define the following terms related to carrier sense multiple access with collision detection scheme

[03 Marks]

a) Carrier sense
b) Multiple access
c) Collision detection

ii.) Draw the cross-sections of the coaxial cable and the optical cable. Mark the relevant parts of each structure clearly.

[07 Marks]

iii.) A transmitter (T) and a receiver (R) are placed between two points A and B as shown in Figure 2, that are separated with a distance between A and B = 10km, signal attenuation = 2 dB per km, transmitting voltage 1V, receiver threshold level 0.2V. Calculate the minimum gain of the amplifiers (A) shown in Figure 2. Assume that each amplifier has the same gain.

[10 Marks]

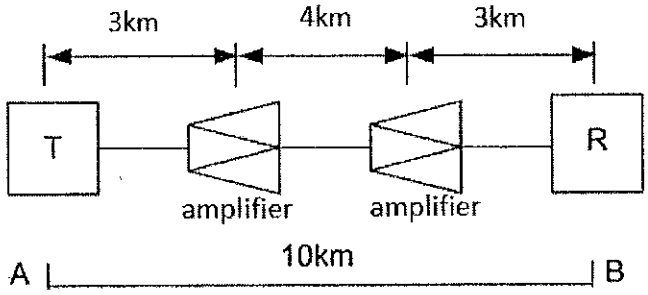


Figure 2

Appendix

ISA of Accumulator Architecture

Mnemonic	Syntax	Operation	Description	Add Mode	Flags affected
Arithmetic instructions					
ADD	ADD x	Addition	Acc ← Acc + op	#,&,default	ZF, OF, SF, PF =1
SUB	SUB x	Subtraction	Acc ← Acc - op	#,&,default	ZF, OF, SF, CF, PF =1
MUL	MUL x	Signed multiplication	Acc (16 bit) ← Acc(8 LSBs) * op(8 LSBs)	#,&,default	ZF, SF, PF =1. OF, CF=0
DIV	DIV x	Unsigned division	Acc ← Acc / op2	#,&,default	ZF, SF, PF =1. OF, CF =0
INC	INC	Increment by 1	Acc ← Acc + 1	#,&,default	OF, SF, ZF, PF=1
Logical instructions					
AND	AND x	Bit-wise And	Acc ← Acc AND op	#,&,default	OF, CF=0; SF, ZF, PF =1
OR	OR x	Bit-wise OR	Acc ← Acc OR op	#,&,default	OF, CF =0; SF, ZF, PF =1
XOR	XOR x	Bit-wise XOR	Acc ← Acc XOR op	#,&,default	OF, CF=0; SF, ZF, PF =1
SHL	SHL	Shift left by 1-bit	CF ← Acc (MSB), op← Acc (14 down to 0) & 0	Implied (A)	CF= bit shifted by Acc. SF, ZF, PF=1.
SHR	SHR	Shift right by 1-bit	CF ← Acc (LSB), Acc ← 0 & Acc (15 down to 1)	Implied (A)	CF= bit shifted by Acc. SF, ZF, PF=1.
ROL	ROL	rotate left by 1-bit	CF ← Acc (MSB), op← Acc (14 down to 0) & CF	Implied (A)	CF= bit shifted by Acc. SF, ZF, PF=1.
ROR	ROR	rotate right by 1-bit	CF ← Acc (LSB), Acc ← CF & Acc (15 down to 1)	Implied (A)	CF= bit shifted by Acc. SF, ZF, PF=1.
NOT	NOT	One's compliment negation	op1 ← NOT Acc	Implied (A)	none
Control Transfer instructions					
Conditional Branches					
JC	JC d	Jump if carry	If CF =1 then PC ← PC + Operand	PC relative	none
JOF	JOF d	Jump if over-flow	If OF =1 then PC ← PC + Operand	PC relative	none
JS	JS d	Jump if Sign	If SF =1 then PC ← PC + Operand	PC relative	none
JP	JP d	Jump if parity	If PF =1 then PC ← PC + Operand	PC relative	none
JZ	JZ d	Jump if result is zero	If ZF =1 then PC ← PC + Operand	PC relative	none
Unconditional branch					
JUMP	JUMP d	Jump	PC ← PC + Operand	PC relative	none
Loops					
LOOZ	LOOZ d	Loop until zero	Count ← Count – 1, IF Count =0; Loop termination ELSE; PC ← PC + operand	PC relative	none
Calls and Returns					
CALL	CALL d	Procedure call	implied return address ← PC, PC ← immediate address	*	none
RETURN	RETURN	Return from procedure	PC ← Contents of implied return address	**	none
Miscellaneous instructions					
NOP	NOP	No operation		none	none
Data Movement instructions					
LOADacc	LOADacc AM,d	Copy the operand to the accumulator	Immediate: Acc ← op; Direct: Acc ← memory (op)	#, default	none
STOREacc	STOREacc AM,d	Copies the accumulator to the memory address	Direct: Memory (op) ← Acc Indirect, Memory {memory (op)} ← Acc	Default, &	none

*Immediate operand is used as the jumping location.

**Contents of the implied return address is used as the jumping location

x- Memory Address or immediate value, d- Displacement

Addressing Modes -AM

Immediate	#
Direct	default
Indirect	&