The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering

091

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**:EEX5351 Digital Electronic Systems**
Academic Year	: 2021/22
Date	: 19th February 2023
Time	: 0930-1230hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper contains two (2) questions in SECTION A and four (4) questions in SECTION B on **eight (8)** pages.
3. Answer all questions in SECTION A.[60 Makrs], and answer any Two questions from SECTION B.[40 Marks].
4. Answer for each question should commence from a new page.
5. Refer to the Annexure of the VHDL syntax given in page five(5) to write VHDL code, if any.
6. Refer to the Annexure of the D-FLIP-FLOP datasheet in page six (6) to design the circuits, if required.
7. This is a Closed Book Test(CBT).
8. Answers should be in clear handwriting.

9.Do not use Red colour pen, and clearly state your assumptions if any

Section A: Answer ALL questions [60 Marks]

Idle stop-start control unit(ISSCU)

The following description is about the idle Stop-Start (ISS) control unit in a motor vehicle where it shuts off the engine whilst the vehicle is stationary and executes vehicle functions through secondary battery power. The ISS mode can be switched on/off by using the ISS button. This system involved parts like the gasoline engine, electric Integrated Starter/Generator(ISG), and battery. When the engine is running and the vehicle is moving, idle-stop is affected after stepping on the brake and the vehicle is stopped; the idle-stop is get activated and the ISG unit will stop the engine. The idle-start will quickly re-start the engine, which stopped under idle-stop when the brake pedal is released or the steering wheel is turned. The Idle-stop is getting activated only when the vehicle speed is gone over 20km/h. The Idle-stop will stop the engine by setting the engine conditions where the engine gets quickly re-started from idle-start than normal/regular start-stop engine condition. (The ISG is using the battery power to start/stop the engine. Ones the engine is running; it turns the engine's movement into power by directly connecting with engine).

[Q1]

(i) Identify the inputs and outputs of the ISSCU and draw a block diagram to show how ISSCU is get integrated with sensors, actuators, and other subunits.

[5 marks]

(ii) Draw the Moor-type Finite state machine (FSM) state diagram for the ISS controller.

[7 marks]

(iii) Draw the ASM chart for the ISSCU, and clearly show the input, output, and states.

[8 marks]

(iv) Draw the circuit diagram using D Flip-flops and other necessary components. Clearly explain the working procedure of the ISSCU, indicating the internal functionality of the controller. Cleary shows how the controlling is made and the data paths.

[20 marks]

(v) Write the complete VHDL code for the design ISSCU and include comments where necessary.

[10 marks]

[Q2]

(i) Briefly explain the terms controllability and observability on digital system design for testability (DFT) and list techniques that could apply to improve the testability of ISSCU.

[5 marks]

(ii) Write a VHDL testbench code to illustrate how to perform a functional-level fault model for the ISSCU. Generate test cases/set for testbench by indicating purpose of each test.

[5 marks]

Section B: answer any two questions. [40 Marks]

[Q3]

A Septenary (base-7 Heptimal) number system counts from 1 to 6 which can be displayed on the 3-segment LED display depicted in Fig3.1. A LED is illuminated when the corresponding input A, B, and C is asserted high.

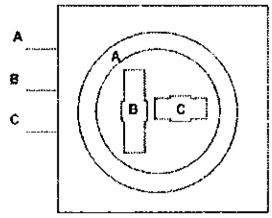


Figure 3.1: 3-segemnt display

Figure 3.2:A Septenary number sequence(staring lowest from left to highest on the right)

The LED patterns for the six digits of the Septenary number system are shown in Fig3.2, where the illuminated segments are shaded. The numbers are ordered from lowest to highest with the lowest number on the left, and the highest on the right.

(*Note: Refer the D-flip-flop datasheet todo the design, if required*)

(i) Draw a state diagram to an up-counter based on the Septenary number system described above. **Encode the count as a 3-bit value corresponding to the input pattern required on the 3-segment display**. The count sequence should cycle from the lowest to the highest number and then reset back to the lowest.

[5 marks]

(ii) Briefly explain how to design this counter to operate properly under don't care conditions.

[3 marks]

(iii) Draw the circuit diagram of Q3.(i) for the outputs that drive the display as a self-starting up-counter by including required signals and using D-FF.(*show the circuit derivation steps*).

[12 marks]

[Q4]

(i) Express A'B+ AB +BC as the sum of minterms and product of Maxterms. Your answers should be in the shorthand notation $\Sigma_m()$ and $\prod_M()$. Draw the circuit for $\Sigma_m()$ function.

[4 marks]

(ii) Implement the Q4(i) expression with a minimal number of 2:1 multiplexers and no other logic. Assume that only A, B, and C are available and not their complements.(*Do not reduce the Boolean expression*)

[6 marks]

(iii) Show how fault detected on Q4(i) circuit using path sensitized test and identify the complete test set TS={}. (Draw a table and clearly show the path, sensitized apply and fault detection).

[10 marks]

[Q5]

Figure 5 depict a positive edge-triggered sequential circuit that has inputs (X, Reset, CLK) and output(Z). It initializes with the S0 state as "00". *(Refer to the D-flip flop datasheet to answer questions. if required and needs to mention, under what condition data has been extracted).*

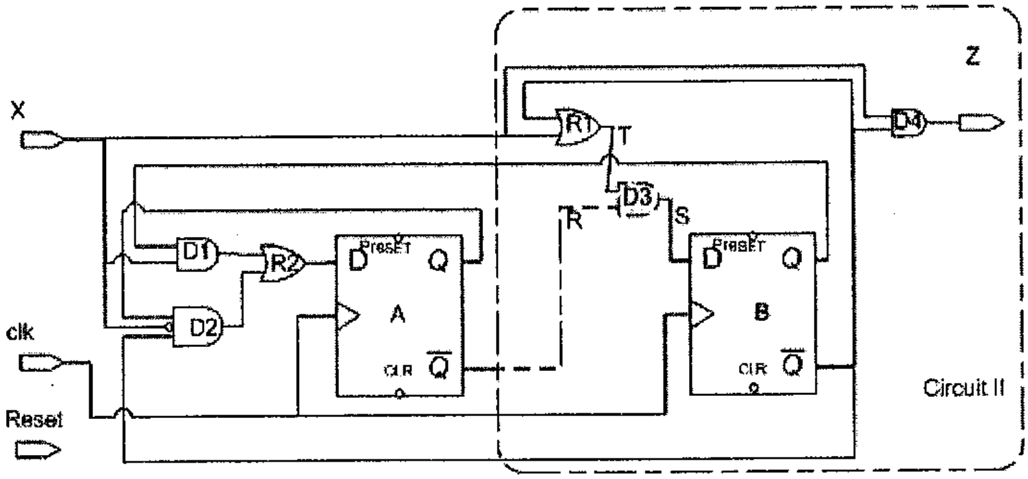


Figure 5.1:A Sequential Circuit Diagram

(i) Considering there is a 13ns delay on each gate, compute the propagation delay of the circuit Fig5.1.

[4 marks]

(ii) Show how to implement the asynchronous **reset** function operation on fig(5) circuit. The Reset signal needs to be set high to reset the circuit to its initial state.

[3 marks]

(iii) Considering the modified Fig. 5.1:**circuit II** diagram depicted in Fig. 5.2 and add Reset function define on Q5(ii).Draw the timing diagram for the following description. Show the X, CLK, Reset, Qb, Z, and other necessary signals.

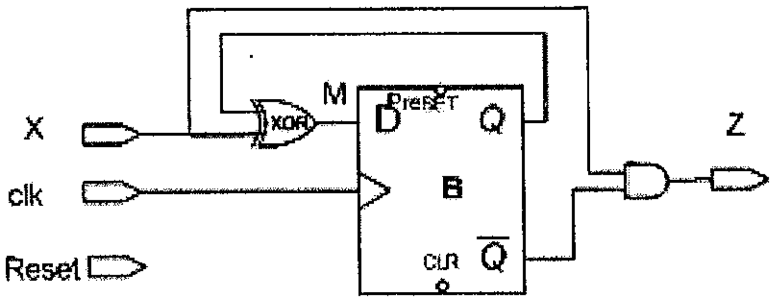


Figure 5.2: New Circuit II Diagram

Assume that the following signals are initialized at time zero as; Reset with low, and X, CLK, and Qb with high. The Reset signal is low for 5ns, next high for 30ns, and then zero again. The X input is high for 105ns, and low again. Calculate the duration of Z output active high using the timing diagram after the Reset. *(Assume all the gates have zero delays and refer to the D-FF datasheet for other delays if required).*

[13 marks]

[Q6]

The sequence detector detects the sequence in the following description. There is a synchronized reset, P as input and Q as output, when the Reset is high output Q becomes low and initializes the detector. When Reset is removed, it requires two changes in P to set Q to be high and two changes in P to set Q to be low again. The output changes on the next positive clock edge with respect to the input changes. Reset and P are shown at the rising edge of the clock in Table 6. (Assume P is low when reset is high to reduce the complexity and have zero delays in the circuit).

Table 6: Example behavior of the sequence detector Finite Sequence Machine (FSM)

Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
P	0	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	0
Q	0	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1

(i) Identify the FSM type that produces the Table 6 output and draw a state diagram for the sequence detector. Briefly describe the nature of the sequence.

[7 marks]

(ii) Draw the basic configurations of the programmable read-only memory.

[2 marks]

(iii) Specify the truth table for a ROM which would realize the same function in Q6(i). Clearly show the size of the ROM.

[5 marks]

(iv) Implement the combinational circuit part of the sequence detector as a ROM-based circuit. Show how the D-FF IC pins should be connected to the ROM circuit. *(refer to the D-FF datasheet for D-FF IC pin configuration, if required).*

[6 marks]

Annexure

Syntax of selected instructions of the VHDL

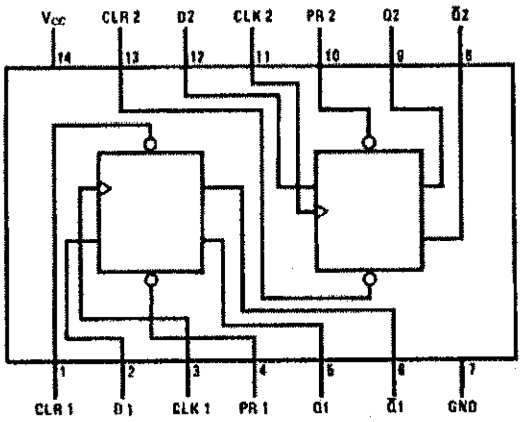
```
⌧ ARCHITECTURE architecture_name OF entity_name IS
    [declaration part]
  BEGIN
    Concurrent statements part
  ENDarchitecture_name
⌧ CASE expression IS
    WHEN value=>statements;
    WHEN value=>statements;
  WHEN OTHERS statements;
  END CASE;
⌧ COMPONENT component_name
  PORT (port1_name :port1_type;
  port2_name :port2_type;
          …);
  END COMPONENT [component_name];
⌧ ENTITY entity_name IS
  PORT (port1 :port1_type;
  port2 :port2_type;
          …);
  END entity_name;
⌧ IF condition THEN
    Sequence of statements
    {ELSIF condition THEN
       Sequence of statements}
  [ELSE
    Sequence of statements]
  END IF;
⌧ LIBRARY library_name;
⌧ Instance_label: component_name PORT MAP (first_port, second_port,
                                              third_port, …);
  Instance_label: component_name PORT MAP (formal1=>actual1,
                                             formal1=> actual1,
                                             formal1=> actual1, …);
⌧ [process_label:] PROCESS (signal1, signal2, …)
                       [declaration part]
  BEGIN
  Sequential statements part
  END PROCESS;
⌧ SIGNAL signal_name :signal_type;
⌧ TYPE type_name;
⌧ USE library_name.type_expression.inclussion;
⌧ WAIT FOR time_expression;
  WAIT ON signal1, signal2, …;
  WAIT UNTIL condition;
⌧ WHILE condition LOOP
    Sequential statements
  END LOOP;
```

DM74LS74A
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is LOW or HIGH without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram



Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going Transition
Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25		35	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		30		35	ns

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 3)		0		25	MHz
f_{CLK}	Clock Frequency (Note 4)		0		20	MHz
t_W	Pulse Width (Note 3)	Clock HIGH	18			ns
		Preset LOW	15			ns
		Clear LOW	15			ns
t_W	Pulse Width (Note 4)	Clock HIGH	25			ns
		Preset LOW	20			ns
		Clear LOW	20			ns
t_{SU}	Setup Time (Note 3)(Note 5)		20↑			ns
t_{SU}	Setup Time (Note 4)(Note 5)		25↑			ns
t_H	Hold Time (Note 5)(Note 6)		0↑			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 3: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$, and $V_{CC} = 5V$.

Note 4: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$, and $V_{CC} = 5V$.

Note 5: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 6: $T_A = 25°C$ and $V_{CC} = 5V$.