The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX5536 Computer Architecture**
Academic Year	: 2021/2022
Date	: 21st of February 2023
Time	: 1330 – 1630hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **Eight (8)** questions on **Eight (8)** pages.
3. Answer **any five (5)** questions. All questions carry equal marks.
5. Answer for each question should commence from a new page.
6. This is a Closed Book Test **(CBT).**
7. Answers should be in clear handwriting.
8. Do not use red colour pens.

Question 1

A computer is constructed using a 3.6 GHz processor. It is integrated with 512 MB RAM, which has 1.5 ns latency. The processor has three types of instructions: Branch, Arithmetic & Logic, and Memory Move. The processor needs 5, 4, and 5 clocks to execute each type of instruction, respectively. Of all the instructions executed, 20% are Branch instructions, and 40% are Arithmetic and Logic operations. Branch and Memory Move instructions need two memory access, but Arithmetic and Logic instructions need only one.

i.) Calculate the average CPI of the processor. **[03 marks]**
ii.) Find the MIPS rating of the processor. **[04 marks]**
iii.) Calculate the MIPS rating of the computer. **[08 marks]**
iv.) Estimate the time taken to execute a program with n number of instructions. **[05 marks]**

Question 2

A design of an instruction execution path has L logic delays. So, it will take L time to execute an instruction in a one-stage pipeline. However, the logic path can be divided into many stages. In the multistage pipeline, it is assumed that logic delay L is equally subdivided. Accordingly, in each stage, the minimum clock period is calculated as
$T_{clock} = t_{max} + \tau$; where t_{max} is approximated to the largest delay of a stage, and τ is the sum of the setup time of a latch and clock skew. Let k as the length of the instruction sequence and s as the number of stages.

(i) What is the clock period T_{clock} in terms of $\boldsymbol{L}$, $\boldsymbol{s}$ and $\boldsymbol{\tau}$? **[02 marks]**
(ii) What is the execution time of the $\boldsymbol{k}$ number of instructions? **[04 marks]**
(iii) Derive an equation to calculate the optimum number of stages in the pipeline. **[08 marks]**
(iv) Prove the minimum execution time of $\boldsymbol{k}$ number of instructions is $(\sqrt{L} + \sqrt{\tau(k-1)})^2$ **[08 marks]**

Question 3

i.) The throughput of a pipeline is inversely proportional to the bottleneck of the pipeline. Explain the statement. **[04 marks]**
ii.) An instruction execution path will take 9ns to execute an instruction in a one-stage pipeline. However, this logic path can be divided into any number of stages, and the logic delay (9ns) can also be subdivided equally. Moreover, the sum of the setup time of a latch and clock skew will be 1ns. Let s as the number of stages. Assume that the pipeline receives a set of instructions without branching instructions.
   a) What is the clock period T_{clock} in terms of s? **[06 marks]**
   b) What is the execution time of 101 instructions? **[04 marks]**
   c) Calculate the optimum number of stages that the pipeline should have for a minimum execution time of 101 instructions. **[06 marks]**

Question 4

Specification of a hard disk of 1.2 GB made up of several platters is given as follows: 620 cylinders, 64 heads, and 63 sectors. The performance measuring utility shows the average seek time as 9ms. Disk rotational speed is calculated as 3600 rpm.

(i) Define the terms seek time and rotational delay. **[02 marks]**

(ii) Calculate the number of bytes in a sector of the hard disk. (Note: bytes in a sector should be the nearest to the power of two values) **[02 marks]**

(iii) Calculate the average rotational delay. **[02 marks]**

(iv) How many tracks are there in a cylinder of the disk? **[03 marks]**

(v) Calculate how many tracks are needed to store a file in the size of 3 MB? **[03 marks]**

(vi) What would be the approximate time taken to read a file in the size of 3 MB? **[04 marks]** (Note: assume the file is continuously stored from the 0^{th} sector of the 0^{th} track of any cylinder and the data transfer rate is 1890 kB/s). Consider that the arm may not be positioned on the cylinder where the file is stored before starting to read the file.)

(vii) How many files in size of 3 MB can be saved on that disk? **[04 marks]**

Question 5

(i) Draw typical virtual machine schematics for different styles of Instruction Set Architecture (ISA), i.e. Accumulator, Memory-Memory, Stack, and Load-Store. **[08 marks]**

(ii) Identify the general and special purpose registers in each architecture mentioned above. **[03 marks]**

(iii) What are the addressing modes of the following Intel 8086 instructions?

(a)	MOV AL, BL ;	(AL) ← (BL)	**[03 marks]**
(b)	ADD AL, data ;	(AL) ← (AL) + data	**[03 marks]**
(c)	AND AX, addr ;	(AX) ← (AX) AND (addr)	**[03 marks]**

Note: AL, AX and BL belong to the register set. Here addr is an address of a memory location, and data is a data value.

Question 6

(i) Describe Flynn's classification of computer organization, giving block diagrams for each organization. **[08 marks]**

(ii) Distinguish MIMD multiprocessors from multi-computers or computer networks. **[04 marks]**

(iii) Design an algorithm for the quadric matrix multiplication for a SIMD computer. The number of processor elements (PE) in the SIMD computer is equal to the dimension of the column (or row) of the metrics. Each PE has its own memory, which is large enough to hold three columns of the matrix. **[08 marks]**

Question 7

You are to connect an external device to a computer through the parallel port or the ISA bus. The device accepts a data byte when its *Accept data* pin receives a rising edge of a signal. Immediately the device will set its *data valid* pin to low. As soon as the data byte is written to its memory, the *data valid* pin will be set to high. The device accepts data only when the *data valid* pin is high.

i.) Draw a block diagram to show the connectivity of the device with the computer through the parallel port (Appendix A) or ISA bus (Appendix B). Indicate which pins of the parallel port or the ISA bus you will connect with the device's pins.

[06 marks]

ii.) Draw a typical timing diagram for data transferring from the computer to the device.

[04 marks]

iii.) Give an algorithm for sending a byte to the device from the computer. You must show all values used for configuring the ISA bus (values for the address bus and the data bus) or the parallel port (addresses and values of the relevant ports) each time they are used.

[06 marks]

iv.) Expand your algorithm to send a file to the device. **[04 marks]**

Question 8

A hierarchical Cache – Main Storage memory subsystem has the following specifications: cache access time of 50ns, the main storage access time of 500ns, 80% of memory requests are for read, hit ratio of 0.9 for read access and the Write Through policy is employed. Estimate the following.

i.) The average access time of the system, considering only the memory read cycle. **[06 marks]**

ii.) The average access time of the system both for read and write requests. **[08 marks]**

iii.) The hit ratio, considering the write cycle. **[06 marks]**

Appendix A

Parallel port connector description

Pin: D-sub	Signal	Function	Source	Register		Inverted at con-nector?	Pin: Centron-ics
				Name	Bit #		
1	nStrobe	Strobe D0-D7	PC[1]	Control	0	Y	1
2	D0	Data Bit 0	PC[2]	Data	0	N	2
3	D1	Data Bit 1	PC[2]	Data	1	N	3
4	D2	Data Bit 2	PC[2]	Data	2	N	4
5	D3	Data Bit 3	PC[2]	Data	3	N	5
6	D4	Data Bit 4	PC[2]	Data	4	N	6
7	D5	Data Bit 5	PC[2]	Data	5	N	7
8	D6	Data Bit 6	PC[2]	Data	6	N	8
9	D7	Data Bit 7	PC[2]	Data	7	N	9
10	nAck	Acknowledge (may trigger interrupt)	Printer	Status	6	N	10
11	Busy	Printer busy	Printer	Status	7	Y	11
12	PaperEnd	Paper end, empty (out of paper)	Printer	Status	5	N	12
13	Select	Printer selected (on line)	Printer	Status	4	N	13
14	nAutoLF	Generate automatic line feeds after carriage returns	PC[1]	Control	1	Y	14
15	nError (nFault)	Error	Printer	Status	3	N	32
16	nInit	Initialize printer (Reset)	PC[1]	Control	2	N	31
17	nSelectIn	Select printer (Place on line)	PC[1]	Control	3	Y	36
18	Gnd	Ground return for nStrobe, D0					19,20
19	Gnd	Ground return for D1, D2					21,22
20	Gnd	Ground return for D3, D4					23,24
21	Gnd	Ground return for D5, D6					25,26
22	Gnd	Ground return for D7, nAck					27,28
23	Gnd	Ground return for nSelectIn					33
24	Gnd	Ground return for Busy					29
25	Gnd	Ground return for nInit					30
	Chassis	Chassis ground					17
	NC	No connection					15,18,34
	NC	Signal ground					16
	NC	+5V	Printer				35

[1]Setting this bit high allows it to be used as an input (SPP only)

[2]Some Data ports are bidirectional.

Parallel port register definitions

Base address: 0378h

Data Register (Base Address)

Bit	*Pin: D-sub*	Signal Name	Source	Inverted at connector?	Pin: Centronics
0	2	Data bit 0	PC	no	2
1	3	Data bit 1	PC	no	3
2	4	Data bit 2	PC	no	4
3	5	Data bit 3	PC	no	5
4	6	Data bit 4	PC	no	6
5	7	Data bit 5	PC	no	7
6	8	Data bit 6	PC	no	8
7	9	Data bit 7	PC	no	9

Some Data ports are bidirectional. (See Control register, bit 5 below.)

Status Register (Base Address +1)

Bit	*Pin: D-sub*	Signal Name	Source	Inverted at connector?	Pin: Centronics
3	15	nError (nFault)	Peripheral	no	32
4	13	Select	Peripheral	no	13
5	12	PaperEnd	Peripheral	no	12
6	10	nAck	Peripheral	no	10
7	11	Busy	Peripheral	yes	11

Additional bits not available at the connector:
0: may indicate timeout (1=timeout).
1, 2: unused

Control Register (Base Address +2)

Bit	*Pin: D-sub*	Signal Name	Source	Inverted at connector?	Pin: Centronics
0	1	nStrobe	PC[1]	yes	1
1	14	nAutoLF	PC[1]	yes	14
2	16	nInit	PC[1]	no	31
3	17	nSelectIn	PC[1]	yes	36

[1]When high, PC can read external input (SPP only).
Additional bits not available at the connector:
4: Interrupt enable. 1=IRQs pass from *nAck* to system's interrupt controller. 0=IRQs do not pass to interrupt controller.
5: Direction control for bidirectional Data ports. 0=outputs enabled. 1=outputs disabled; Data port can read external logic voltages.
6,7: unused

Appendix B

ISA (Industry Standard Architecture) Bus

Pins layout

D	Description	Name	Pin	Pin	Name	Description	D
/	Ground	GND	B1	A1	IO CHK	I/O Channel Check	-I
O	Reset	RESET	B2	A2	SD7	System Data bit 7	I/O
/	Power +5V	+5V	B3	A3	SD6	System Data bit 6	I/O
I	Interrupt Request 9	IRQ9	B4	A4	SD5	System Data bit 5	I/O
/	Power -5V	-5V	B5	A5	SD4	System Data bit 4	I/O
I	DMA Request 2	DRQ2	B6	A6	SD3	System Data bit 3	I/O
/	Power -12V	-12V	B7	A7	SD2	System Data bit 2	I/O
/	Zero Wait State	0WS	B8	A8	SD1	System Data bit 1	I/O
/	Power +12V	+12V	B9	A9	SD0	System Data bit 0	I/O
/	Ground	GND	B10	A10	IO RDY	I/0 Channel Ready	-I
O	System Memory Write	SMEMW	B11	A11	AEN	Address Enable	O
O	System Memory Read	SMEMR	B12	A12	SA19	System Address bit 19	O
I/O	I/O Write	IOW	B13	A13	SA18	System Address bit 18	O
I/O	I/O Read	IOR	B14	A14	SA17	System Address bit 17	O
O	DMA Request Acknowledge 3	DACK3	B15	A15	SA16	System Address bit 16	O
I	DMA Request 3	DRQ3	B16	A16	SA15	System Address bit 15	O
O	DMA Request Acknowledge 1	DACK1	B17	A17	SA14	System Address bit 14	O
I	DMA Request 1	DRQ1	B18	A18	SA13	System Address bit 13	O
I/O	Refresh cycle in progress	REFRESH	B19	A19	SA12	System Address bit 12	O
O	System Clock	CLOCK	B20	A20	SA11	System Address bit 11	O
I	Interrupt Request 7	IRQ7	B21	A21	SA10	System Address bit 10	O
I	Interrupt Request 6	IRQ6	B22	A22	SA9	System Address bit 9	O
I	Interrupt Request 5	IRQ5	B23	A23	SA8	System Address bit 8	O
I	Interrupt Request 4	IRQ4	B24	A24	SA7	System Address bit 7	O
I	Interrupt Request 3	IRQ3	B25	A25	SA6	System Address bit 6	O
O	DMA Request Acknowledge 2	DACK2	B26	A26	SA5	System Address bit 5	O
O	T/C	TC	B27	A27	SA4	System Address bit 4	O
?	Buffered Address Latch Enable	BALE	B28	A28	SA3	System Address bit 3	O
/	Power +5V	+5V	B29	A29	SA2	System Address bit 2	O
O	Oscillator	OSC	B30	A30	SA1	System Address bit 1	O
/	Ground	GND	B31	A31	SA0	System Address bit 0	O

Signal Description

CLOCK (*System Drive*) output
The system clock is a synchronous microprocessor cycle clock.

RESET (*Reset Drive*) output
This signal goes high at power-up, hardware reset, or when low line-voltage occurs.

SA0 to SA19 (*System Addresses*) input/output
The system address lines run from bit 0 through 19. They are latched onto the falling edge of BALE.

SD0 to SD7 (*System Data bits*) Input/Output
System data bits 0 to 7.

BALE (*Buffered Address Latch Enable*) input
The buffered address latch enable is used in latch SA0 to SA19 on the falling edge of BALE. During DMA cycles, BALE is forced high.

IO CHK (*I/O Channel Check*) active low input
I/O channel check is active low signal which indicate that a parity error exists in the I/O board.

IO RDY (*I/O Channel Ready*) input
This signal lengthens I/O or memory cycles and should be held low with valid addresses. It can be held low for a maximum of 2.5 microseconds.

IRQ 3 to 7, 9 (*Interrupt Requests*) input
These interrupt request signals indicate I/O service request attention. They are prioritized in the following sequences: highest IRQ 9 and lowest IRQ 3, 4, 5,6,7,8.

IOR (*I/O Read*) active low input/output
Instructs an I/O device to drive its data onto the data bus.

IOW (*I/O Write*) active low output
Instructs an I/O device to read the data off the data bus.

SMEMR (*System Memory Read*) output
The system memory read signal is low while the low first megabyte memory is being read.

SMEMW (*System Memory Write*) output
The system memory write signal is low while the low first megabyte memory is being written.

DRQ 0 to 3 (*DMA Requests*) active high input
DMA Request channels 0 to 3 are for 8-bit data transfers. DRQ4 is used on the system board. Hold a DRQ line high until its DMA Request Acknowledge (DACK) goes active. Their priority is in the following sequences: highest DRQ 0,1,2, and 3.

DACK 1 to 3 (*DMA Request Acknowledges*) output
These signals are used to acknowledge the corresponding signals for DRQ 0 to 3.

AEN (*Address Enable*) output
The address enable is high when the DMA controller drives the address bus and is low when the CPU drives the address bus.

REFRESH (*Refresh cycle in progress*) active low input/output
This signal indicates a refresh cycle is in progress.

TC (*T/C*) output

OSC (*Oscillator*) output
The oscillator signal is used for the color graphic card.
High-speed clock (70 ns, 14.31818 MHz), 50%duty cycle

0WS (*Zero Wait State*) input
The zero wait state indicates to the microprocessor that the present bus cycle can be completed without inserting any additional wait cycles.