

The Open University of Sri Lanka  
Faculty of Engineering Technology  
Department of Electrical & Computer Engineering



Study Programme	: Bachelor of Software Engineering Honours : Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	: EEX5563 EEX5564 Computer Architecture and Operating Systems
Academic Year	: 2021/2022
Date	: 21 <sup>st</sup> of February 2023
Time	: 1330 – 1630hrs
Duration	: 3 hours

### General Instructions

1. Read all instructions carefully before answering the questions.
  2. This question paper consists of **Eight (8)** questions on **Five (5)** pages.
  3. Answer **any five (5)** questions. All questions carry equal marks.
  5. Answer for each question should commence from a new page.
  6. This is a Closed Book Test (CBT).
  7. Answers should be in clear handwriting.
  8. Do not use red colour pens.
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### Question 1

A computer is constructed using a 3.6 GHz processor. It is integrated with 512 MB RAM, which has 1.5 ns latency. The processor has three types of instructions: Branch, Arithmetic & Logic, and Memory Move. The processor needs 5, 4, and 5 clocks to execute each type of instruction, respectively. Of all the instructions executed, 20% are Branch instructions, and 40% are Arithmetic and Logic operations. Branch and Memory Move instructions need two memory access, but Arithmetic and Logic instructions need only one.

- i.) Calculate the average CPI of the processor. [03 marks]
- ii.) Find the MIPS rating of the processor. [04 marks]
- iii.) Calculate the MIPS rating of the computer. [08 marks]
- iv.) Estimate the time taken to execute a program with n number of instructions. [05 marks]

### Question 2

- i.) List what needs to be considered to allocate or deallocate memory in a dynamic partition memory allocation system. [06 marks]
- ii.) Write an algorithm in pseudo-code to allocate and deallocate memory blocks for a dynamic partition memory allocation system considering the list you have given above. [06 marks]
- iii.) Draw a flowchart to implement the working of the virtual memory with segmentation. [08 marks]

### Question 3

- i.) State the difference between preemptive and non-preemptive scheduling algorithms and give examples for each. [02 marks]
- ii.) What is the advantage of having different time-quantum sizes on different levels of a multilevel queuing system? [02 marks]
- iii.) Consider a system running ten I/O-bound tasks and one CPU-bound task. Assume that the I/O bound tasks issue an I/O operation once for every two milliseconds of CPU computing and that each I/O operation takes 20 milliseconds to complete. Also, assume that the context switching overhead is 0.1 milliseconds and that all processes are long-running tasks. Calculate the CPU utilization for a round-robin scheduler when;
  - a) The time quantum is 1 millisecond [05 marks]
  - b) The time quantum is 10 milliseconds [05 marks]
- iv.) Suppose that a scheduling algorithm favours the processes that have used the least processor time in the recent past. Why will this algorithm favour I/O-bound programs and yet not permanently starve CPU-bound programs? State all the assumptions. [06 marks]

#### Question 4

Specification of a hard disk of 1.2 GB made up of several platters is given as follows: 620 cylinders, 64 heads, and 63 sectors. The performance measuring utility shows the average seek time as 9ms. Disk rotational speed is calculated as 3600 rpm.

- (i) Define the terms seek time and rotational delay. [02 marks]
- (ii) Calculate the number of bytes in a sector of the hard disk. (Note: bytes in a sector should be the nearest to the power of two values) [02 marks]
- (iii) Calculate the average rotational delay. [02 marks]
- (iv) How many tracks are there in a cylinder of the disk? [03 marks]
- (v) Calculate how many tracks are needed to store a file in the size of 3 MB? [03 marks]
- (vi) What would be the approximate time taken to read a file in the size of 3 MB? [04 marks]  
(Note: assume the file is continuously stored from the 0<sup>th</sup> sector of the 0<sup>th</sup> track of any cylinder and the data transfer rate is 1890 kB/s). Consider that the arm may not be positioned on the cylinder where the file is stored before starting to read the file.)
- (vii) How many files in size of 3 MB can be saved on that disk? [04 marks]

#### Question 5

- i.) What are the process scheduling criteria? Describe them briefly. [06 marks]
- ii.) Consider the following set of processes in the table below, with the length of the CPU-burst time given in milliseconds.

Job	Arrival Time	CPU-Burst Time	Priority
A	0	5	5
B	0	2	2
C	4	3	1
D	5	3	7
E	8	1	4
F	15	2	1
G	16	3	4
H	17	1	3
I	18	4	6

A smaller priority number implies a higher priority. Draw four Gantt charts that illustrate the execution of these processes using First Come First Served, Shortest Job Next, Non-preemptive Priority, and Round Robin scheduling. Choose the proper quantum size for Round Robin scheduling and clearly state your assumptions. [10 marks]

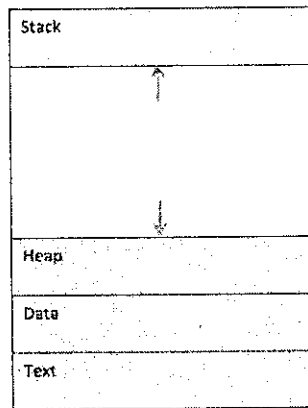
- iii.) Calculate the average turnaround time for each method used above and compare them. [04 marks]

### Question 6

- (i) Describe Flynn's classification of computer organization, giving block diagrams for each organization. [08 marks]
- (ii) Distinguish MIMD multiprocessors from multi-computers or computer networks. [04 marks]
- (iii) Design an algorithm for the quadric matrix multiplication for a SIMD computer. The number of processor elements (PE) in the SIMD computer is equal to the dimension of the column (or row) of the metrics. Each PE has its own memory, which is large enough to hold three columns of the matrix. [08 marks]

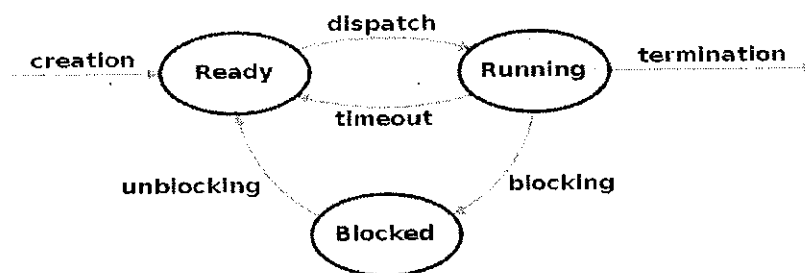
### Question 7

- i.) The following *Figure 7.1* shows a simplified layout of a process inside the main memory. Briefly explain what is loaded in each section. [04 marks]



*Figure 7.1: A simplified layout of a process inside the main memory*

- ii.) Briefly explain the states of a process referring to the given "Process state diagram", as depicted in Figure 7.2. [06 marks]



*Figure 7.2: Process state diagram*

- iii.) State the importance of having a "Process Control Block (PCB)". [04 marks]
- iv.) Differentiate a "Thread Control Block (TCB)" from a "Process Control Block (PCB)". [06 marks]

### Question 8

A hierarchical Cache – Main Storage memory subsystem has the following specifications: cache access time of 50ns, the main storage access time of 500ns, 80% of memory requests are for read, hit ratio of 0.9 for read access and the Write Through policy is employed. Estimate the following.

- i.) The average access time of the system, considering only the memory read cycle. **[06 marks]**
- ii.) The average access time of the system both for read and write requests. **[08 marks]**
- iii.) The hit ratio, considering the write cycle. **[06 marks]**



