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THE OPEN UNIVERSITY OF SRI LANKA

Faculty of Engineering Technology
Department of Electrical & Computer Engineering
Bachelor of Technology Honours in Engineering
FINAL EXAMINATION – (2016/2017)

ECX6236 – PROCESSOR DESIGN

Time Allowed: **3 hours**

Date: 02 December 2017 **Time: 0930 – 1230 hours**

INSTRUCTIONS TO CANDIDATES

1. This question paper contains four questions in **SECTION A** and four questions in **SECTION B** on 5 pages.
2. Answer **ALL FOUR** questions in **SECTION A.** [70 Marks]
3. Answer any **TWO** questions from **SECTION B.** [30 Marks]

NOTE:

1. When you have to write VHDL Program for your answer, provide appropriate comments where necessary.

2. Refer annexure for syntax of VHDL instructions in page 5 when you answer the questions in this paper.

3. State your assumptions (if any) clearly.

Continued...

SECTION A:

Answer ALL questions. [70 Marks]

Processor for Search Operation (PSO)

Read the following scenario (as shown by italic). You are required to analyze and design the requirements of the ***PSO*** given below according to the given specifications.

The Department of Motor Traffic (DMT) will be going to introduce windshield stickers with a Radio Frequency Identification (RFID) tag to identify the vehicles. The windshield sticker will include a passive RFID tag. This will enable a reader to obtain basic information such as the registration number, the chassis number, fuel, year of registration and province. Based on this information, the reader can request if it wishes to do so, any further information that it requires on a particular vehicle through the DMT. The system can be utilized for effective self-parking systems (Reference: Sunday Observer, 05 November 2017).

To serve this purpose, it is required to manufacture a special hardware module to improve the performance of searching the vehicle information. The special hardware module consists with a special processor for searching operation (PSO), a Special Unit (SU) for reading the UHF Gen 2 passive RFID tag information of the vehicles, and Database (DB) as an external storage module (SD card).

Your task is to design a special processor – (PSO), which can be fabricated later. PSO is used as only for this purpose and your design may be differ from general purpose processor.

The ISA (Instruction Set Architecture) of PSO should be capable enough to develop a necessary program (codes) for the above application. Your ISA should provide basic operations related to database searching, reading the passive RFID tag information of the vehicles and other necessary operations. You may need a special memory (cache memory) to retrieve a portion of the database with vehicle information (assume that the database is given to you) and other digital logic devices.

The SU has SOR (Start of Reading) signal, EOR (End of Reading) signal, and DATA buffer (char (24)). PSO needs to give low to high pulse to SOR in order to activate reading the RFID tag of the vehicle. Once the SOR signal has been sent, the PSO needs to wait until EOR signal is available to read the tag data (EPC). EOR signal will be high to low after SU reads the RFID tag of the vehicle and ready to send the tag data (EPC). After EOR signal becomes available, PSO can read the RFID tag data from the DATA buffer of the SU. UHF Gen 2 passive RFID tag includes EPC (Electronic Product Code) memory bank, which holds the char (24) EPC code (As an example, 3575BCD15BC614E000000001).

DATA buffer value needs to be searched in the DB and if it is found then set a flag (name DF) in the PSO else clear the flag DF in the PSO. Assume that the DB has two columns (ID, EPC) and initially it has only 100 vehicle information.

Since the DB is available as the external storage module (SD card), you may assume it will release the EPC once it received the ID value. For an example, if you are given 50 as ID to this module, it will release the EPC related to ID=50.

The designed processor must be simple. You may include other additional hardware units/components align with the scenario. State all other assumptions clearly (if any), when you are answering the following questions.

[Q1]

(a) Draw a diagram and show how to deploy the PSO (once it is fabricated) for developing special hardware module for the given application. (Do not need to design the special hardware module but need to show the inputs and the outputs of the PSO related to the EU with the DB). [10 Marks]

(b) Briefly describe the operation of the diagram drawn in Q1.(a) indicating internal functionality of PSO. [05 Marks]

[Q2]

(a) Tabulate the required instructions of PSO and design the ISA to fulfill the given specifications. [15 Marks]

(b) Using the ISA designed in Q2.(a), write a simple program to access the vehicle information from the given database according to the EPC. [05 Marks]

[Q3] Draw a Block diagram for the PSO. Clearly state all functions of each block inside the processor and show the data path. Indicate all input/output signals of the PSO. [15 Marks]

[Q4]

(a) Identify the entities for which you need to write VHDL codes to synthesize the PSO. [05 Marks]

(b) Write behavioral/structural VHDL codes for each entity except for the control unit of the PSO. (You may define the control unit as a component.) [15 Marks]

SECTION B:

Answer any TWO questions. [30 Marks]

[Q5]

(a) Construct a state diagram of the control unit of the PSO in Section A [10 Marks]

(b) Draw an ASM chart of the control unit based on the state diagram drawn in Q5.(a). [05 Marks]

[Q6]

(a) Construct the sub-unit which produces the following timing diagram shown in Figure Q6 using suitable digital logic gates and a Flip Flop. Clearly show the input and output signals of each component. [08 Marks]

(b) Write structural VHDL codes for the constructed sub-unit in Q6.(a). [07 Marks]

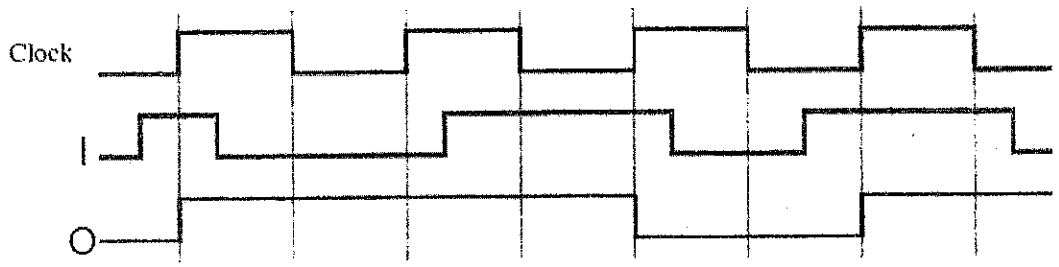

Figure Q6: Timing Diagram (I: Input, O: Output)

[Q7]

(a) Briefly explain the factors that should be considered for estimating the price of the PSO designed in Section A. [08 Marks]

(b) Estimate performance (in CPI) of the PSO designed in Section A. [07 Marks]

[Q8]

(a) Briefly describe the task of a processor designer. [07 Marks]

(b) Briefly describe the steps need to follow to design a hardwired control unit of a processor. [08 Marks]

Annexure

Syntax of selected instructions of the VHDL

☒
```
ARCHITECTURE architecture_name OF entity_name IS
  [declaration part]
```

☒
```
BEGIN
  Concurrent statements part
END architecture_name
```

☒
```
CASE expression IS
   WHEN value=> statements;
   WHEN value=> statements;
   WHEN OTHERS statements;
END CASE;
```

☒
```
COMPONENT component_name
  PORT (port1_name : port1_type;
        port2_name : port2_type;
        …);
END COMPONENT [component_name];
```

☒
```
ENTITY entity_name IS
  PORT (port1 : port1_type;
        port2 : port2_type;
        …);
END entity_name;
```

☒
```
IF condition THEN
  Sequence of statements
  {ELSIF condition THEN
     Sequence of statements}
[ELSE
  Sequence of statements]
END IF;
```

☒
```
LIBRARY library_name;
```

☒
```
Instance_label: component_name PORT MAP (first_port, second_port,
                                         third_port, …);
Instance_label: component_name PORT MAP (formal1=> actual1,
                                         formal1=> actual1,
                                         formal1=> actual1, …);
```

☒
```
[process_label:] PROCESS (signal1, signal2, …)
                   [declaration part]
                 BEGIN
                   Sequential statements part
                 END PROCESS;
```

☒
```
SIGNAL signal_name : signal_type;
```

☒
```
TYPE type_name;
```

☒
```
USE library_name.type_expression.inclussion;
```

☒
```
WAIT FOR time_expression;
WAIT ON signal1, signal2, …;
WAIT UNTIL condition;
```

☒
```
WHILE condition LOOP
  Sequential statements
END LOOP;
```