THE OPEN UNIVERSITY OF SRI LANKA
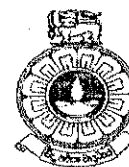## Faculty of Engineering Technology
Department of Electrical & Computer Engineering

Bachelor of Technology Honors in Engineering

Final Examination (2016/2017)
ECX6151: Digital Electronics Systems

Date: 18ᵗʰ November 2017 (Friday)	**Time:** 9:30 am – 12:30 am

Answer all the parts in Section I.
Answer any two questions from Section II, each worth of 20 marks.
Maximum marks that can be obtained from Section I and Section II are 60 and 40 respectively.

SECTION I

Q1. Consider the two-player game described below. There are six buttons placed in three rows as shown in Figure 01. Each time a player takes turns in removing a button. The player who picks up the last button wins the game. The rules for playing are as follows:

Rule01: Each player should pick a button from the row containing the largest number of buttons.
Rule02: If there are three rows with equal number of buttons, then, the player should pick from the last row.
Rule03: If only two rows have equal number of buttons and in each more than one button, then, the player should pick a button from the second row. Else, the player can pick from any row.
Rule04: If any incorrect move occurs, the game restarts.

Based on the above information,

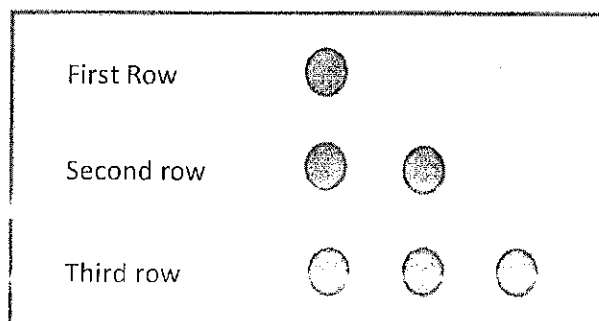|		
(i)	State the inputs and the outputs	(05 marks)
(ii)	Draw the state transition diagram.	(20 marks)
(iii)	Compute the ASM chart.	(15 marks)
(iv)	Write the VHDL code to implement the design.	(30 marks)

Figure01

SECTION II

Q2. Error detection is a necessity to ensure reliable digital communications over unreliable channels. Parity check is a well-established method to detect errors by adding extra bits to the transmitted data. Consider a parity generator which adds a parity bit to message with three bits and transmits. The parity generator ensures even number of '1's (even parity) in the transmitted message. At the receiver, considering the received message the parity checker declares if there is an error in transmission if the number of '1's is an odd number.

    (i)   Write the Boolean expression for the function of the parity generator.   (02 marks)

    (ii)   Compute the truth table for the (a) parity checker and (b) parity generator.   (06 marks)

    (iii)   Draw the logic gate circuits for the (a) parity checker and (b) parity generator.   (06 marks)

    (iv)   Draw the pin connection diagram to realize the (iii) (a) and (iii) (b) using 7486 IC (see Figure02).   (06 marks)

Q3. (i)   Write the truth table for the encoding for the numbers from 0 to 9.   (03 marks)

    (ii)   Compute the decimal indications for the given pulse trains shown in Figure03.   (03 marks)

    (iii)   Design a counter using T flop flops which counts the sequence 000, 010, 100, 110 and resets back to 000.

        a. Draw the simplified state diagram and the excitation table for the counter.   (06 marks)

        b. Compute the simplification using an appropriate technique and draw the logic circuit diagram.   (08 marks)

Q4. (i) Draw the basic configurations of the following.   (06 marks)

        (a) Programmable read only memory

        (b) Programmable array logic

        (c) Programmable logic array

    (ii)   Implement the three input functions F1, F2, F3 using a ROM.   (06 marks)

        $F1(a,b,c) = \Sigma(0,2,3,7)$, $F2(a,b,c) = \Sigma(1,4,6,7)$, $F3(a,b,c) = \Sigma(2,5,6)$,

    (iii)   Design a combinational circuit using a ROM. The circuit accepts a three bit binary number and computes the square of the input number.   (04marks × 2)

        (a) Draw the truth table for the above function.

        (b) Design a circuit to realize the above function.

Q5. (i)   Implement the following function using a multiplexer.   (06 marks)

        $F(A,B,C,D) = \Sigma(0,1,3,4,8,9,15)$

    (ii)   Write the complete behavioral VHDL code to implement a full adder.   (06 marks)

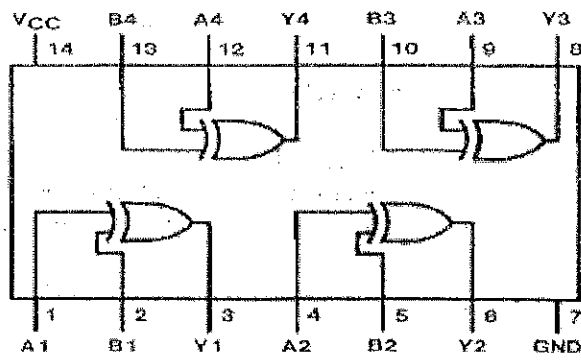   (iii)   Design a full adder circuit using an appropriate decoder and OR gates. Clearly mention the size of the decoder.   (08 marks)
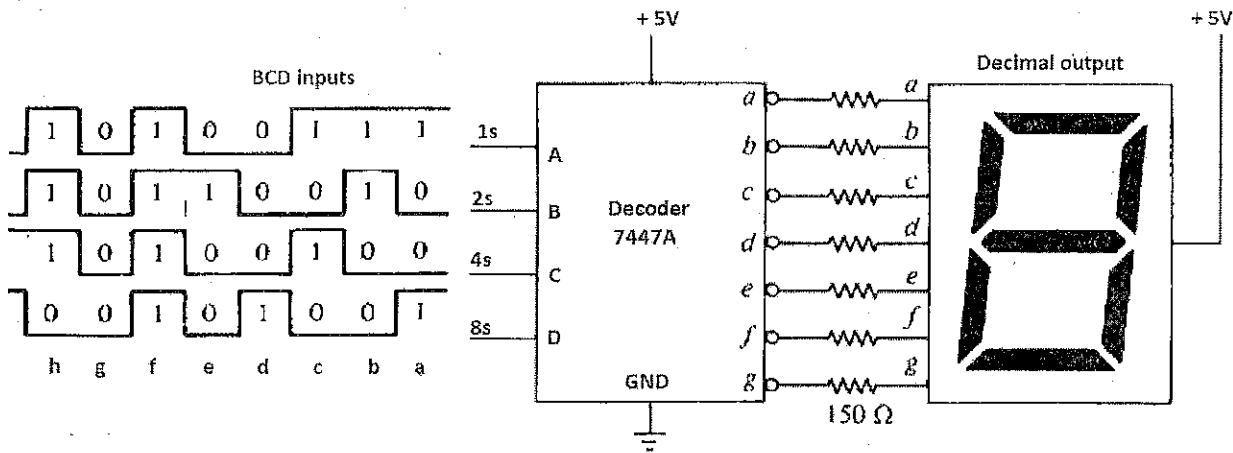
Figure02 - Pin diagram of 7486 IC

Figure03