The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical & Computer Engineering

CQ3

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX4530/EEX4230- Fault Diagnosis in Electronic Circuits**
Academic Year	: 2021/2022
Date	: 10th March 2023
Time	: 0930-1230hrs

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **eight (8)** questions on **eight (08)** pages.
3. Answer any **Five (5)** questions only. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. This is a Closed Book Test (CBT).
6. Answers should be in clear handwriting.
7. **Do not** use a red colour pen.
8. Adhere to usual notations.

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1. A single-stage amplifier circuit is shown in Figure 1. I_{DSS} =10mA, $V_{GS(off)}$ = -3V

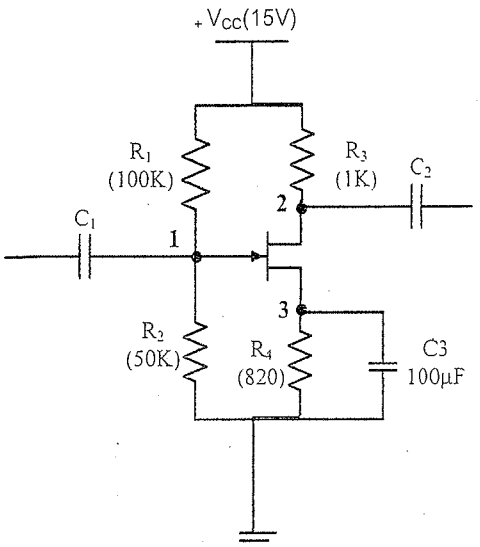

Figure 1

a. Calculate,
   i. Gate voltage
   ii. Drain current
   iii. Gate source voltage [06 Marks]

b. Calculate the test point voltages. [02 Marks]

c. Find the faulty component/s and the type of the fault, giving reasons. [12 Marks]

Case	TP 1(V)	TP 2(V)	TP 3(V)	Symptom
A	5	7.91	5.81	Low gain
B	5	15	0	No output
C	5	7.91	5.81	No output

2. A single-stage transistor amplifier(Collector to base bias) is shown in Figure 2. The current gain of the transistor is 50.

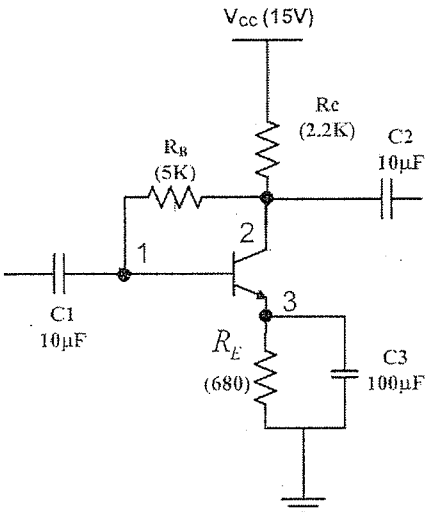

Figure 2

a. Calculate the voltages of test points 1,2, and 3 at no signal condition. [06 Marks]

b. The table given below shows the voltages at test points under faulty conditions. Find the faulty components and the type of the faults giving reasons. [08 Marks]

Case	TP 1(V)	TP 2(V)	TP 3(V)	Symptom
A	15	15	14.3	No output
B	0	15	0	No output
C	1.9	11	1.2	No output
D	3.9	4.4	3.2	Low Gain

c. Calculate the test point voltages when BE is Short circuited. [06 Marks]

3.

a. State the advantages and disadvantages of linear regulators over switch mode regulators. [03 Marks]

b. A DC power supply is shown in Figure 3.

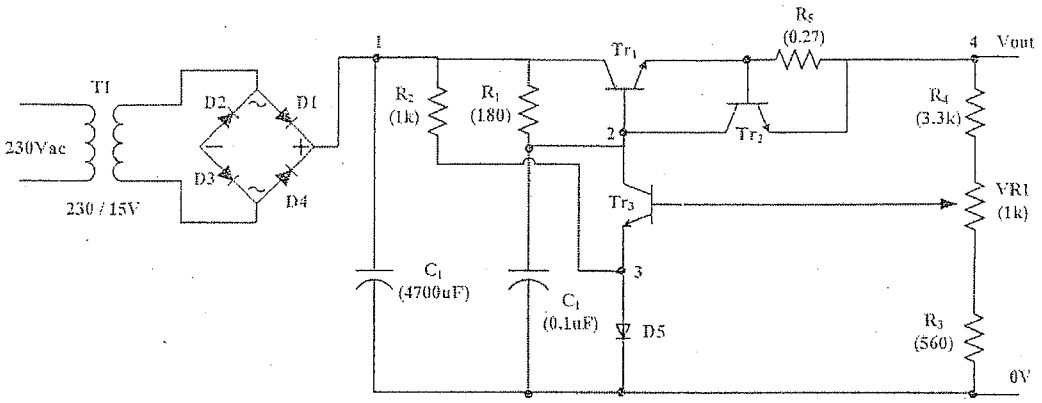

Figure 3

i. Calculate the range of the output voltage. [03 Marks]

ii. Is it possible to use this supply for a 27W load at 9V? If not, show how you are going to modify the circuit to achieve this. [04 Marks]

iii. The following table shows the voltages at the test points under faulty conditions. Find the faulty component/s with fault type giving reasons. Assume VR1 is set to give the maximum output. [10 Marks]

Case	TP 1(V)	TP 2(V)	TP 3(V)	TP 4(V)
A	15.0	14.80	0.60	14.20
B	15.0	6.96	0.60	6.36
C	15.0	5.81	0	5.21
D	15.0	14.80	0	14.20
E	15.0	15.0	0.60	0

4.

a. An amplifier of open loop A_o is supplied with positive feedback. If the feedback ratio is β, find an expression for overall gain. [03 Marks]

b. What will happen when $\beta A_o = 1$? [02 Marks]

c. A blocking oscillator is shown in the following Figure 4.

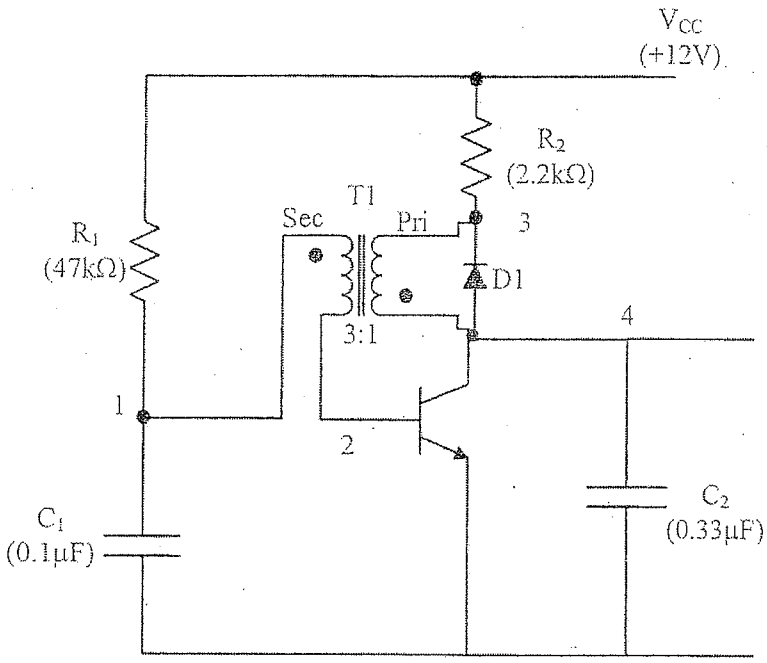

Figure 4: Blocking Oscillator

i. Explain the operation of the above oscillator and sketch the waveforms at the output. [04 Marks]

ii. State the function of D1. [02 Marks]

iii. The following table shows the DC voltages at test points under faulty conditions. Identify the faulty components indicating reasons. [09 Marks]

Case	TP 1(V)	TP 2(V)	TP 3(V)	TP 4(V)	Symptom
A	0	0	12	12	No output
B	0.7	0.7	0.1	0.1	No output
C	9.7	0	12	12	No output

5. Consider the DC voltage regulator circuit shown in Figure 5.

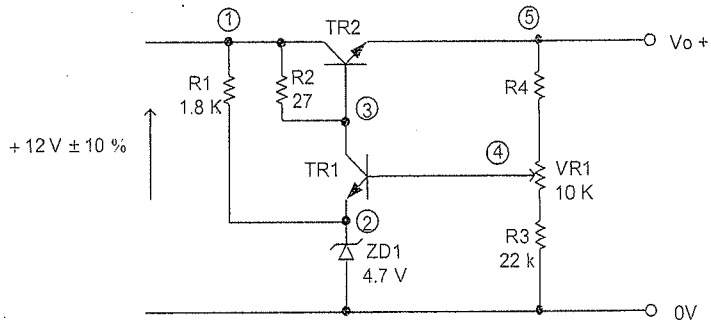

Figure 5: DC voltage regulator

Assume that the current gain of TR2 and V_{CE} (min) is 30V and 1V, respectively. The transistor TR1 is of high gain type.

(i) Find a suitable value for R4 to obtain the maximum guaranteed output voltage and calculate it for this value of R4. [03 Marks]

(ii) Find the minimum output voltage. [02 Marks]

(iii) Calculate the guaranteed maximum load current. [02 Marks]

(iv) Calculate the maximum power dissipation in TR2, R2, and ZD1. [03 Marks]

(v) Show the active current limit circuit implementation for this power supply and find the component values for the worst-case maximum load current. [02 Marks]

(vi) The following table shows the test point voltages under fault conditions. Determine the faulty component/s with fault type giving reasons. Assume VR1 is set for the maximum output voltage. [08 Marks]

Case	TP1	TP2	TP3	TP4	TP5	Symptom
A	12.00	4.700	11.82	6.140	11.22	no regulation
B	12.00	4.700	10.28	5.300	9.680	max. load current = 0.9A
C	12.00	4.700	5.900	5.300	5.300	no regulation
D	12.00	4.700	12.00	0	0	no output

6.

a. Draw a basic block diagram of an oscillator circuit. [02 Marks]

b. State the factors that are causing frequency instability in the oscillator. [04 Marks]

c. Figure 6 shows a Wien bridge oscillator circuit. Transistors used in Figure 6 have high current gains.

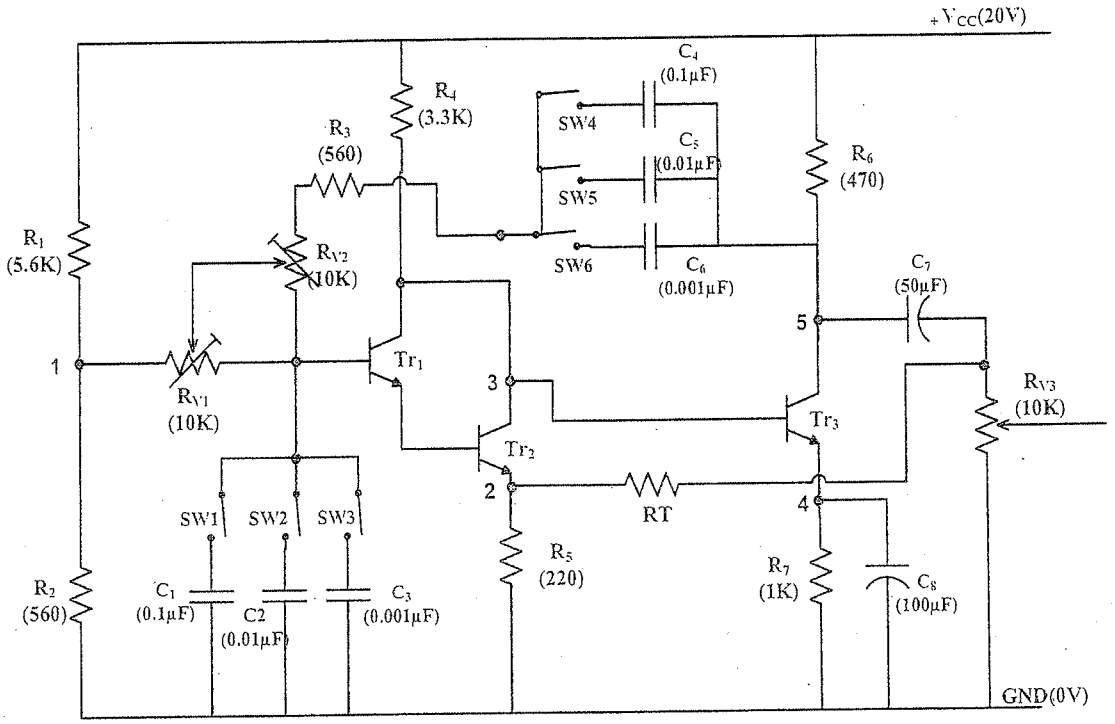

Figure 6: Wien Bridge Oscillator

i. Calculate the possible output frequency ranges in the circuit. [01 Mark]
ii. Calculate the test point voltages shown in figure 6. (State necessary assumptions) [04 Marks]
iii. Find the fault and the faulty components for the following cases. [09 Marks]

Case	TP 1(V)	TP 2(V)	TP 3(V)	TP 4(V)	TP 5(V)	Symptom/s
A	1.8	0.1	18.8	18.2	18.3	No output
B	1.8	0.6	10.6	10.0	15.2	No output with the change in switching position
C	10.7	9.5	9.6	9.0	9.1	No output

7. A DC amplifier circuit is shown in Figure 7.

a. Write the type of feedback used in this amplifier circuit and state the path of the feedback. [02 Marks]
b. Calculate the test point voltages at no signal. (Assume that Tr1 and Tr2 are matched pairs of transistors) [08 Marks]
c. Calculate the voltage gain of this circuit. [02 Marks]

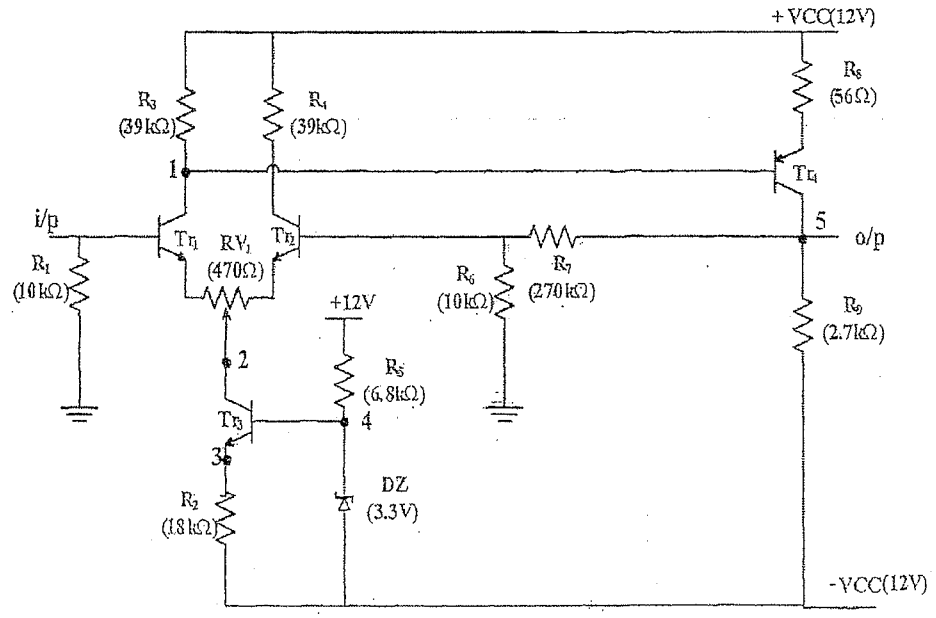

Figure 7

d. Find the fault component/s giving reasons. [08 Marks]

Fault	TP1(V)	TP2(V)	TP3(V)	TP4(V)	TP5(V)
P	11.9	-0.9	-9.3	-8.7	-12.0
Q	12.0	5.6	5.8	6.4	-12.0
R	11.8	-0.9	-9.3	-8.7	-12.0
S	11.4	-0.9	-9.3	-8.7	-12.0

8. Consider the multivibrator circuit shown in Figure 1. The transistors may be assumed as high gain and $V_{CE}(sat) = 0$.

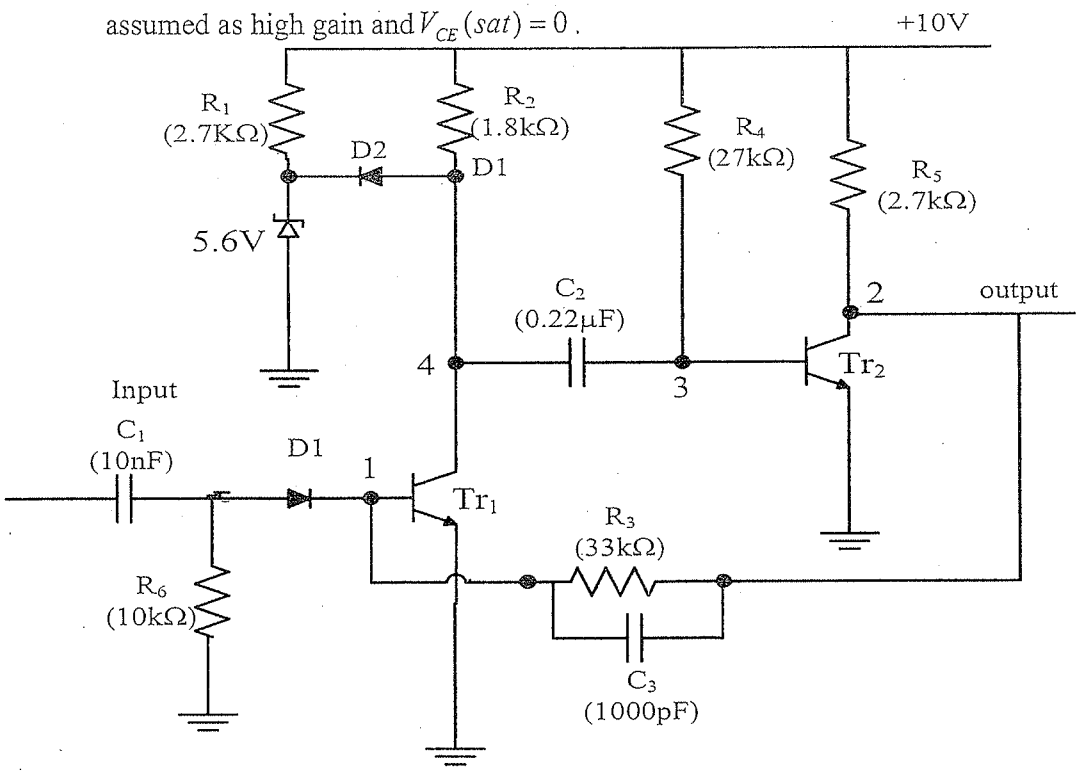

Figure 8

a. By giving reasons, identify the type of multivibrator shown in Figure 8.
[02 Marks]

b. Calculate the test point voltages when there is no input signal and find the collector current in each transistor. [06 Marks]

c. A pulse train of short duration, having an amplitude of 8V is applied to the input. Draw the resulting waveforms at each test point on a common time scale. Calculate and mark important voltage and time values on your sketch.
[06 Marks]

d. Under fault conditions, all test point voltages are observed before applying any input. Then the test points are observed by an oscilloscope after applying a narrow test pulse of 8V. Some of the results observed are listed below. Find the faulty component/s indicating the fault type with reasons. [06 Marks]

Case	TP1	TP2	TP3	TP4	Symptom/s
A	0.0	0.0	0.7	0.7	No output
B	0.0	0.0	0.7	6.2	No output pulse; negative pulse at TP3
C	0.0	0.0	0.7	6.2	Output pulse width> Normal

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