THE OPEN UNIVERSITY OF SRI LANKA
DEPARTMENT OF COMPUTER SCIENCE
BSC DEGREE PROGRAM – 2024/2025
FINAL EXAMINATION
CSU5306: DIGITAL ELECTRONICS
DURATION: TWO HOUR (2 HOURS)

Date: 15.12.2024 **Time: 1.30pm - 3.30pm**

General Instructions

1. Read all instructions carefully before answering the questions.

2. This question paper consists of 06 questions on 04 pages.

3. Answer any 04 questions only. All questions carry equal marks.

4. The answer for each question should commence from a new page.

5. Draw fully labeled diagrams where necessary.

6. Involvement in any activity that is considered an exam offense will lead to punishment.

7. Use blue or black ink to answer the questions.

8. Clearly state your index number in your answer script.

Q1.

The Smart Irrigation System on a farm is equipped with three types of sensors—Sensor A, Sensor B, and Sensor C, and they are used to monitor critical environmental conditions that directly affect crop growth. These sensors measure **soil moisture**, **air temperature**, and **wind speed**, providing logical outputs based on the readings. The system triggers a warning signal whenever certain conditions become unfavorable for the crops, helping the farm manager proactively protect the plants.

Sensor	Condition	Logical Value	Explanation
Sensor A (Soil Moisture)	Soil moisture < 30% (dry soil)	1 (active)	Irrigation required due to dry soil.
	Soil moisture ≥ 30% (sufficiently moist)	0 (inactive)	Soil is sufficiently moist, no irrigation needed.
Sensor B (Air	Temperature > 35°C	1 (active)	Temperature exceeds safe

Temperature)	(high/unsafe)		limit for crops.
	Temperature ≤ 35°C (safe)	0 (inactive)	Temperature is within safe range for crops.
Sensor C (Wind Speed)	Wind speed > 15 km/h (strong wind)	1 (active)	Wind speed is high, potentially harmful to crops.
	Wind speed ≤ 15 km/h (calm wind)	0 (inactive)	Wind speed is low, less likely to cause damage.

The smart irrigation system is programmed to trigger a warning signal under two specific conditions. **Condition 1** occurs if either of the following happens:

1. The soil moisture falls below 30%, indicating that the soil is too dry, and irrigation is needed.
2. The temperature exceeds 35°C and the wind speed rises above 15 km/h, which together could pose a significant risk to crop health due to excessive heat and potential wind damage.

Alternatively, **Condition 2** triggers the warning signal when both of the following conditions are met:

1. The soil moisture is below 30%, signaling dry soil that needs irrigation.
2. The temperature exceeds 35°C, creating a potentially dangerous combination of dry soil and high temperatures that could stress the crops.

The smart irrigation system ensures that the farm closely monitors environmental factors and provides a warning signal whenever conditions deviate from the optimal range for crop health. These warnings allow the farm manager to take corrective action, such as adjusting irrigation schedules or preparing crops for extreme weather events, like high temperatures or strong winds, thus ensuring better care and higher crop yields.

i. Derive the Truth Table for the above scenario.

ii. Derive the simplified Boolean equation for the above scenario using K-maps.

iii. Draw the circuit for the above (ii) simplified equation.

iv. Derive the POS from the (i) truth table and simplify it using Boolean rules

Q2.

i. Convert the following binary numbers to decimal numbers
   a. 101101.1001
   b. 111000101.1101

ii. Convert the following decimal numbers to binary numbers.
   a. 392.250
   b. 64.75

iii. Conver the following words into ASCII code.State the code in hexadecimal and binary. (Use the ASCII Table given in the Annex 1, at the end of the paper)
"Forest cover has decreased by 30% since 1990."

iv. Prove the following Boolean Algebra rules.
   a. Associative law
   b. Identity law

Q3.

i. Explain the function of clocked JK Flip Flop. (Use Block diagrams, Logic Diagrams, and Timing Diagrams as needed)

ii. Explain the propagation delay in Asynchronous circuits.

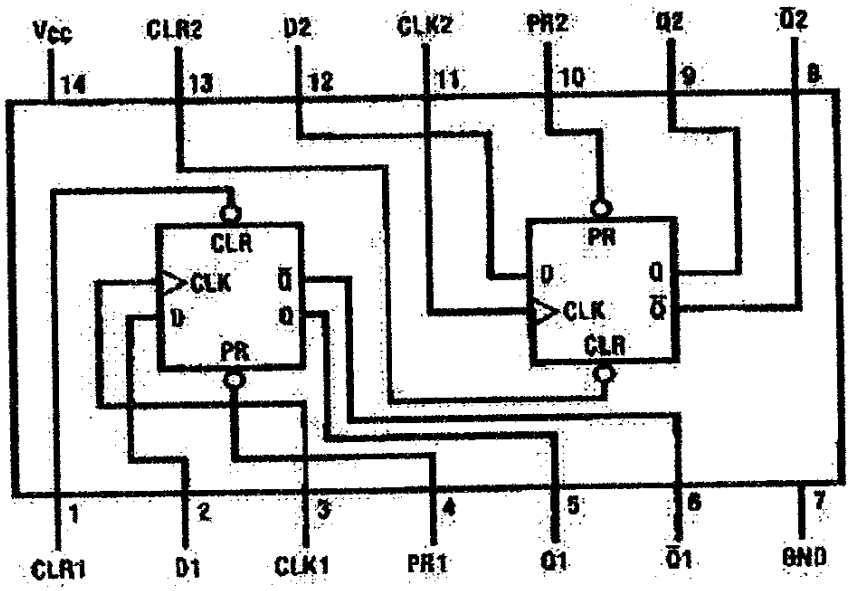
iii. Design the timing diagram of the Walking Ring Counter.

iv. Explain the difference between Clear and Reset pulse in counters.

Q4.

i. The D flip-flop has two main specified inputs, Preset and Clear. What is the purpose of having them (Preset and Clear) in the D flip-flop?

ii. Build the IC circuit for the 4-bit SIPO(Serial-Input-Parallel-output) Shift Register (hint: Use the following datasheet of the 74HC74 IC).



iii. Name the major two applications of D flip flop.

iv. Draw the Timing Diagram of the above (ii) IC circuit.

Q5.

i. Explain the counting function.

ii. Draw the schematic Diagram (Logic Diagram) to add 101 (base2) and 110 (base2).

iii. Design a block diagram of 16 to 1 Multiplexer using only 4 to 1 Multiplexer.

iv. Design a 1 to 8 Demultiplexer circuit diagram.

Q6.

i. Derive 8-bit RAM using a one-bit memory cell. (Use properly labeled block diagram).

ii. Describe the advantages and disadvantages of the following interaction policies.
   a. Write Back.
   b. Write Through.

iii. Describe the types of ROM.

iv. Design the logic circuit of PAL for the following Boolean function.

A→pq'r + qr

B→pqr's + qr's

C→q's+p'qrs'

D→prs'+pq'r's'+pqr's+qr's

Annex 1

00	NUL	10	DLE	20	SP	30	0	40	@	50	P	60	`
01	SOH	11	DC1	21	!	31	1	41	A	51	Q	61	a
02	STX	12	DC2	22	"	32	2	42	B	52	R	62	b
03	ETX	13	DC3	23	#	33	3	43	C	53	S	63	c
04	EOT	14	DC4	24	$	34	4	44	D	54	T	64	d
05	ENQ	15	NAK	25	%	35	5	45	E	55	U	65	e
06	ACK	16	SYN	26	&	36	6	46	F	56	V	66	f
07	BEL	17	ETB	27	'	37	7	47	G	57	W	67	g
08	BS	18	CAN	28	(	38	8	48	H	58	X	68	h
09	HT	19	EM	29	)	39	9	49	I	59	Y	69	i
0A	LF	1A	SUB	2A	*	3A	:	4A	J	5A	Z	6A	j
0B	VT	1B	ESC	2B	+	3B	;	4B	K	5B	[	6B	k
0C	FF	1C	FS	2C	,	3C	<	4C	L	5C	\	6C	l
0D	CR	1D	GS	2D	-	3D	=	4D	M	5D	]	6D	m
0E	SO	1E	RS	2E	.	3E	>	4E	N	5E	^	6E	n
0F	SI	1F	US	2F	/	3F	?	4F	O	5F	_	6F	o

NUL	Null	FF	Form feed	CAN	Cance
SOH	Start of heading	CR	Carriage return	EM	End of
STX	Start of text	SO	Shift out	SUB	Substi
ETX	End of text	SI	Shift in	ESC	Escape
EOT	End of transmission	DLE	Data link escape	FS	File se
ENQ	Enquiry	DC1	Device control 1	GS	Group
ACK	Acknowledge	DC2	Device control 2	RS	Recor
BEL	Bell	DC3	Device control 3	US	Unit se
BS	Backspace	DC4	Device control 4	SP	Space
HT	Horizontal tab	NAK	Negative acknowledge	DEL	Delete
LF	Line feed	SYN	Synchronous idle		
VT	Vertical tab	ETB	End of transmission block		