065

The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering/ Bachelor of Science Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	**: EEX5351 Digital Electronic Systems**
Academic Year	: 2022/23
Date	: 18th February 2024
Time	: 0930-1230hrs
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.

2. This question paper contains two (2) questions in SECTION A and three (3) questions in SECTION B on **six (6)** pages.

3. Answer all questions in SECTION A. [60 Marks], and answer any Two questions from SECTION B. [40 Marks].

4. Answer for each question should commence from a new page.

5. Refer to the Annexure of the VHDL syntax given on page five (5) to write VHDL code, if any.

6. Refer to the Annexure of the D-FLIP-FLOP datasheet on page six (6) to design the circuits, if required.

7. This is a Closed Book Test (CBT).

8. Answers should be in clear handwriting.

9.Do not use Red colour pen, and clearly state your assumptions if any

Section A: Answer ALL questions [60 Marks]

Water Pump Control Unit (WPCU)

The following description gives the water pumping process to overhead tanks installed in three buildings. Water is pumped to those three tanks from a well by a water pump. Your task is to analyse the given description and design the Water Pump Control Unit (**WPCU**) controller using digital electronic components.

Design specification of the control unit,

- Water ***level sensors*** are installed inside the water tank and send a signal to indicate the tank's water level, either low or full. The water pump will pump the water from the well to the empty overhead tanks until **they get** full.
- ***Solenoid valves*** control the water pumping upstream line for each overhead tank (*default, All closes*).
- ***Leakage sensors*** are placed on each building to detect if there is a leakage or not. The water pump will pump water when there is no leakage.
- ***ON/OFF switches*** on each building activate or deactivate the water pumping process temporarily for the respective building.
- ***Reset switch*** resets the **WPCU**.

[Q1]

(i) Identify the inputs and outputs of the **WPCU** and draw a block diagram to show how the **WPCU** is integrated with sensors, actuators, and other subunits. [5 marks]

(ii) Identify the special functional units/circuits and other necessary components in the **WPCU** and draw a block diagram to show their interconnections. Clearly explain the working procedure of the **WPCU**, indicating the internal functionality of the controller. [14 marks]

(iii) Draw the Mealy-type Finite state machine (FSM) diagram for the **WPCU** control unit. [07 marks]

(iv) Draw the Timing diagram for Q1)(iii) control unit. [07 marks]

(v) Draw the circuit diagram using T Flip-flops and other necessary components. [07 marks]

(vi) Write the complete VHDL code for the design **WPCU** and include comments where necessary. [10 marks]

[Q2]

(i) Briefly explain the terms controllability and observability on digital system design for testability (DFT) and show how you integrate the scan flip-flops to improve the testability of the **WPCU** circuit. [5 marks]

(ii) Write a VHDL testbench code to illustrate how to perform a functional-level fault model for the **WPCU**. Generate test cases/sets for testbench by indicating the purpose of each test. [5 marks]

Section B: answer any two questions. [40 Marks]

[Q3]

Two (02) bit synchronous counter circuit is depicted in Figure 3. B and C are inputs, and Q0 and Q1 are counter outputs. The respective counter is designed using D-flip flops. The counter operation defines with the D0=(Q0⊕C), D1=[(Q1⊕Q0)⊕D]C+Q1$\overline{C}$ next state functions. The D0 and D1 are inputs of the two D-flip flops in the counter circuit.

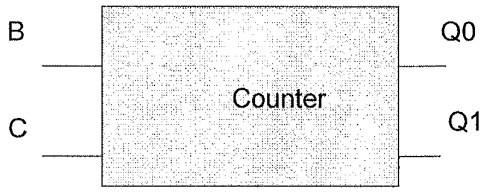


Figure 3:2 bit synchronous counter

(*Note: Refer to the D-flip-flop datasheet to do the design, if required*)

(i) Draw a state transition table of the D0 and D1 functions of the Figure 3 counter circuit. [5 marks]

(ii) Identify the counter sequence and draw a state diagram of the Q3)(i) counter. [5 marks]

(iii) Draw the circuit diagram of Q3)(i) and briefly describe the operation of the counter. [5 marks]

(iv) Considering there is a 15ns delay in each gate compute the propagation delay in Q3)(iii) (Hint: D-Flip Flop timing specification are : T_{PHL}=25, T_{PLH}=30, F=25MHz,T_{su}=20 and T_h=0) [2 marks]

(v) Illustrate how to apply the asynchronous *Reset* using the Q3(iii) counter circuit. Assume the counter resets to "*01*" when *Reset* is applied. [3 marks]

[Q4]

(i) Convert the function F'= $\prod_M(2,4,5)$ to the sum of minterms. Your answers should be in the shorthand notation $\Sigma_m()$. Draw the circuit for the $\Sigma_m()$ function. [4 marks]

(ii) Implement the Q4)(i) $F= \Sigma_m()$ function with a minimal number of 2:1 multiplexers and no other logic. Assume that only A, B, and C are available and not their complements. (*Do not reduce the Boolean expression*) [6 marks]

(iii) Show how fault detected on Q4(i) $F = \Sigma_m()$ circuit using path sensitised test and identify the complete test set TS={}. (Draw a table and show the path, sensitised apply, and fault detection).

[10 marks]

[Q5]

The sequence detector detects the sequence in the following description. There is a synchronised reset; P serves as an input, and Q serves as an output. When the Reset is high, output Q becomes low and initialises the detector. When Reset is low, and if the last three (03) bits from the sequence are "101" then output Q is set to high. If the last three (03) bits are "100" then output Q is locked to 0 thereafter. The output changes on the same positive clock edge with respect to the input changes. Reset and P values are shown at the rising edge of the clock in Table 5. (Assume P is low when Reset is high to reduce the complexity and have zero delays in the circuit).

Table 5: Example behaviour of the sequence detector Finite State Machine (FSM)

Reset	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
P	0	1	1	1	0	1	0	0	1	0	1	0	1	0	1	0	1
Q	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1

(i) Identify the FSM type that produces the Table 5 output and draw a state diagram for the sequence detector. Briefly describe the nature of the sequence.

[10 marks]

(ii) Implement the combinational circuit part of the Q5)(i) sequence detector as a ROM-based circuit. Show how the D-FF IC pins should be connected to the ROM circuit. (*refer to the D-FF datasheet for D-FF IC pin configuration, if required).*

[10 marks]

Annexure

Syntax of selected instructions of the VHDL

```
ARCHITECTURE architecture_name OF entity_name IS
  [declaration part]
BEGIN
  Concurrent statements part
END architecture_name
```

```
CASE expression IS
  WHEN value=>statements;
  WHEN value=>statements;
WHEN OTHERS statements;
END CASE;
```

```
COMPONENT component_name
PORT (port1_name :port1_type;
port2_name :port2_type;
        …);
ENDCOMPONENT [component_name];
```

```
ENTITY entity_name IS
PORT (port1 :port1_type;
port2 :port2_type;
        …);
END entity_name;
```

```
IF condition THEN
  Sequence of statements
  {ELSIF condition THEN
     Sequence of statements}
[ELSE
  Sequence of statements]
END IF;
```

```
LIBRARY library_name;
```

```
Instance_label: component_name PORT MAP (first_port, second_port,
                                          third_port, …);
Instance_label: component_name PORT MAP (formal1=>actual1,
                                         formal1=> actual1,
                                         formal1=> actual1, …);
```

```
[process_label:] PROCESS (signal1, signal2, …)
                    [declaration part]
BEGIN
Sequential statements part
END PROCESS;
```

```
SIGNAL signal_name :signal_type;
```

```
TYPE type_name;
```

```
USE library_name.type_expression.inclussion;
```

```
WAIT FOR time_expression;
WAIT ON signal1, signal2, …;
WAIT UNTIL condition;
```

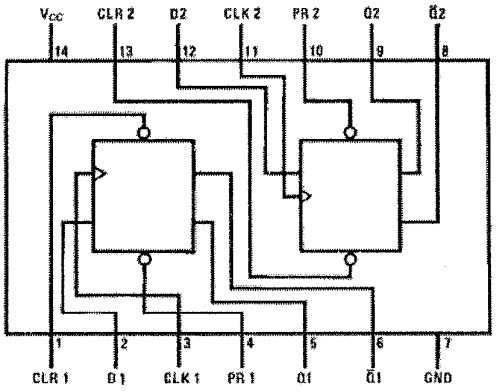
```
WHILE condition LOOP
  Sequential statements
END LOOP;
```

DM74LS74A
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is LOW or HIGH without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram



Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going Transition
Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25		35	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		30		35	ns