037

The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering

Study Programme	: Bachelor of Technology Honours in Engineering
Name of the Examination	: Final Examination
Course Code and Title	: **EEX5536 Computer Architecture**
Academic Year	: 2022/23
Date	: 20th February 2024
Time	: 13:30 – 16:30 hrs.
Duration	: **3 hours**

General Instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of **five (5)** questions in **four (4)** pages.
3. Answer all **FIVE (5)** questions. All questions carry equal marks.
4. Answer for each question should commence from a new page.
5. Answers should be in clear handwriting and do not use Red colour pen.
6. Clearly state your assumptions, if any.
7. This is a **Closed Book Test** (CBT).

Q1

The five stages of the processor have the following latencies (in picoseconds) for an instruction (the multi-cycle and pipelined data-paths):

Fetch (F)	Decode (D)	Execute (EX)	Memory (M)	Writeback (WB)
305 ps	275 ps	280 ps	305 ps	250 ps

*** *Note that these times* ***include*** *the overhead of performing the operation and storing the data in the register needed to save intermediate results between steps.* ***

(a) Compute the *clock period* and *clock rate* for the entire data-path? **[04]**

(b) Assume, there are no hazards or stalls in a pipelined data-path. Compute, how many seconds will it take to execute one instruction? **[04]**

(c) Assuming that *N* instructions are executed, and all *N* instructions are 'add' instructions, what is the speedup of a pipelined implementation when compared to a multi-cycle implementation? Your answer should be an expression that is a function of *N*. **[07]**

(d) Assume you break up the memory stage into 2 stages instead of 1 to improve throughput in a pipelined data-path as below:

F, D, EX, M1, M2, WB

Show how the instructions below would progress through this 6 stages pipeline. Assume, full forwarding hardware is available. **[05]**

	1	2	3	4	5	6	7	8	9	10	11	12	…
lw \$5, 0(\$4)													
add \$7, \$5, \$5													
sub \$8, \$5, \$9													

Q2

(a) Briefly describe two significant drawbacks to obtaining speedup from *N* cores on a multi-core chip (irrespective of finding a good parallel algorithm). **[04]**

(b) Assume that you have a 6-core chip that you want to program to solve a given problem:

- Use as few as 1 core or as many as 6 cores to solve the problem
- The problem requires 450,000 iterations of a main loop to complete
- Each loop iteration requires 100 clock cycles
- Any startup overhead can be ignored (i.e., instructions outside of the loop, to instantiate a new instance of the problem on another core, etc.)

The relation between the communication overhead and the number of cores used to solve the problem as below:

Number of cores used	Communication overhead per iteration
1	0 cycles
2	10 cycles
3	20 cycles
4	30 cycles
5	40 cycles
6	50 cycles

Answers to the following questions. For the above six cases, compute:

i) the communication overhead to complete the main loop; **[03]**

ii) the total execution time to solve the problem and then decide how many cores should be used to solve this problem by explaining the reason. **[08]**

(*Hint: if more than 1 core is used to solve a problem then the communication overhead must be added to the total execution time.*)

(c) Assume that you have 10 cores that you can use to solve the problem in parallel and 98% of your code is parallelizable. Can you get a speedup of 7? If so, how many cores are needed? **[05]**

Q3

(a) Briefly describe two types of cache memory organization in the CPU architecture. **[04]**

(b) Write one advantage and one disadvantage of each organization written in (a). Support each answer with an example and assume that the cache is a direct mapped. **[04]**

(c) Assume the following configuration:

- A processor has a direct mapped cache
- Data words are 8 bits long
- Data addresses are to the word
- A physical address is 20 bits long
- The tag is 11 bits
- Each block holds 16 bytes of data

Compute the number of blocks in this cache. **[06]**

(d) Consider a 16-way set-associative cache with the following configuration:

- Data words are 64 bits long
- Words are addressed to the half-word
- The cache holds 2 Mbytes of data
- Each block holds 16 data words
- Physical addresses are 64 bits long

Compute the number of bits of tag, index, and offset that are needed to support references to this cache. **[06]**

Q4

(a) Briefly explain <u>two types</u> of differences between:

i) the programmed I/O and interrupt initiated I/O. **[04]**

ii) a microprocessor and a micro-program; **[04]**

iii) the hardwired and microprogrammed controls; **[04]**

(b) Figure 1 shows the block diagram of a microprogrammed control unit with the propagation delays (in nanoseconds) between the sub-processes. The CAR is the control address register; ROM is the control memory and CDR is the control data register.

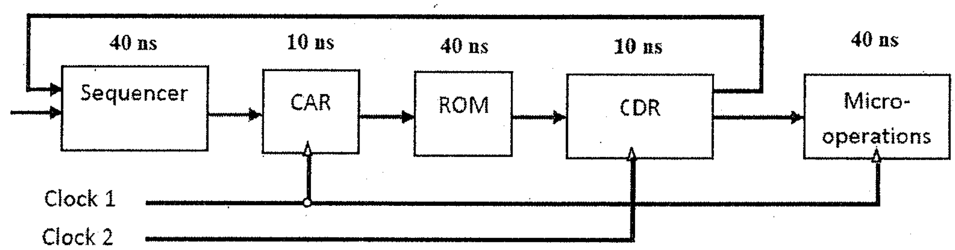

Figure 1: The microprogrammed control unit

i) Briefly describe the process of the microprogrammed control unit. **[04]**

ii) Compute the maximum clock frequency that the control can use. **[02]**

iii) Calculate the clock frequency if the control data register is not used. **[02]**

Q5

Consider a hard disk with a sector size of 512 bytes, 2000 tracks per surface, 50 sectors per track, 5 double-sided platters and average seek time of 10 milliseconds.

Answer the following. Show <u>all the steps</u>:

(a) Compute the track capacity for the disk. **[03]**

(b) Compute the surface capacity for the disk. **[03]**

(c) If disk rotates at 5400 RPM, then approximately what is the maximum rotational delay? **[03]**

(d) If one track can be transferred per rotation, then what is the data transfer rate? **[05]**

(e) Calculate the capacity of the disk. **[06]**

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