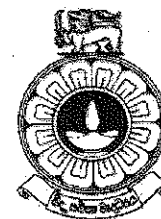


The Open University of Sri Lanka
Faculty of Engineering Technology
Department of Electrical and Computer Engineering



Study Programme	:	Bachelor of Software Engineering Honours/ Bachelor of Science Honours in Engineering
Name of the Examination	:	Final Examination
Course Code and Title	:	EEX5563/ EEX5564 Computer Architecture and Operating Systems
Academic Year	:	2024/25
Date	:	06 th March 2026
Time	:	1400-1700h
Duration	:	3 hours

General instructions

1. **Read all instructions** carefully before answering the questions.
2. Answer **all** questions.
3. This question paper consists of two parts (**Section A** and **Section B**).
4. Part A has twenty (20) MCQ type and Part B has four (04) essay type questions in eight (7) pages
5. Use answer booklet to answer **Section B**
6. Use the sheet provided (page 9) at the end of this exam paper to answer the MCQ questions (**Section A**), remove it and attach it to the **end of the answer** booklet.
7. Answer for each question in **Section B** should commence from a new page.
8. Answers should be in **clear handwriting** and do not use red colour pen.
9. Clearly state your assumptions, if any.
10. Non-programmable calculations are allowed.
11. This is a Closed Book Test (CBT).

Section A [01 Mark x 20 = 20 Marks]

1. What is the main role of an Operating System?
 - a. Compile programs
 - b. Manage hardware and provide services to programs
 - c. Design software
 - d. Control network traffic
2. Which of the following is an example of a process state?
 - a. Ready
 - b. Stored
 - c. Compiled
 - d. Linked

3. Which component of an OS handles CPU scheduling?
 - a. File system
 - b. Scheduler
 - c. Shell
 - d. Loader
4. Which scheduling algorithm gives the CPU to the process with the shortest burst time?
 - a. FCFS
 - b. Round Robin
 - c. SJF
 - d. Priority Scheduling
5. Which of the following is NOT a function of memory management?
 - a. Allocation of memory
 - b. Deallocation of memory
 - c. Address translation
 - d. Virus detection
6. What is a context switch?
 - a. Saving the system to disk
 - b. Switching between two user accounts
 - c. Switching the CPU from one process to another
 - d. Switching from kernel mode to user mode only
7. Which of the following is a non-preemptive scheduling algorithm?
 - a. Round Robin
 - b. Preemptive Priority
 - c. FCFS
 - d. Shortest Remaining Time First
8. What is the main purpose of virtual memory?
 - a. Increase CPU speed
 - b. Increase RAM size physically
 - c. Allow programs larger than physical memory to run
 - d. Improve network speed
9. Which of the following causes deadlock?
 - a. Only one process in the system
 - b. External memory fragmentation
 - c. Circular wait condition
 - d. High CPU speed
10. The kernel is,
 - a. A user application
 - b. The core part of the operating system
 - c. A device driver
 - d. A system utility

11. Which of the following statements about clock rate (clock speed) is correct?
- Clock rate represents the number of instructions a CPU can execute per program.
 - A higher clock rate always guarantees better overall system performance regardless of other factors such as CPI and instruction mix.
 - Clock rate indicates the number of clock cycles generated per second and is typically measured in Hertz (Hz).
 - Clock rate determines the total number of transistors available in a processor.
12. Which of the following statements about **CPU performance metrics** is **incorrect**?
- Execution time is a direct measure of CPU performance, where lower execution time indicates better performance.
 - The CPU clock rate alone is sufficient to accurately compare the performance of two different processors.
 - CPI (Cycles Per Instruction) represents the average number of clock cycles required to execute an instruction.
 - CPU execution time can be calculated using the formula:
$$\text{Execution Time} = \text{Instruction Count} \times \text{CPI} \times \text{Clock Cycle Time}.$$
13. Which of the following statements about Amdahl's Law is incorrect?
- Amdahl's Law assumes the total amount of work (problem size) remains the same when performance is improved.
 - The overall speedup depends on both the part of the program that is improved and the part that is not improved.
 - If the improved part of a program becomes extremely fast, the maximum overall speedup is limited by the part that cannot be improved.
 - Amdahl's Law shows that adding more processors will always give proportional (linear) speedup when the parallel portion is large enough.
14. Which of the following statements correctly describes a hardware-related characteristic of the assembly language used with processors?
- The language abstracts memory management completely, so programmers do not need to consider memory organization.
 - The language is closely tied to the processor's architecture, requiring awareness of registers, memory segmentation, and hardware resources.
 - Programs written in the language can run without modification on any processor regardless of architecture differences.
 - The language automatically manages hardware interrupts without programmer involvement.
15. Which of the following statement about how a processor handles interrupts is correct?
- Interrupts permanently stop the execution of the current program when a subroutine is called.
 - During an interrupt, the processor saves the current execution state and later resumes the original program after completing the subroutine.
 - Subroutine calls using interrupts do not require any mechanism to return to the original program flow.
 - Interrupt-based subroutine calls eliminate the need for modular program design.

16. Which of the following best explains how interrupts improve I/O performance?
- Interrupts force the CPU to continuously check I/O devices to see if they need attention.
 - Interrupts allow the CPU to continue executing other tasks and respond only when an I/O device signals a request.
 - Interrupts prevent multitasking so that I/O operations can complete faster.
 - Interrupts make I/O devices operate without any interaction with the CPU.
17. Which of the following correctly distinguishes write-through and write-back store policies?
- Write-through updates only the cache, while write-back updates both cache and main memory immediately.
 - Write-through updates both cache and main memory immediately, while write-back updates main memory later.
 - Write-through is used only in direct-mapped caches, while write-back is used only in associative caches.
 - There is no performance difference between write-through and write-back policies.
18. Which of the following best explains why cache memory improves system performance?
- Cache memory increases the total size of main memory available to programs.
 - Cache memory stores all program data permanently to avoid accessing main memory.
 - Cache memory stores frequently accessed data closer to the CPU, reducing average memory access time.
 - Cache memory replaces the need for registers inside the CPU.
19. Which of the following statements about memory-mapped I/O is correct?
- I/O devices use a completely separate address space that cannot be accessed like memory.
 - I/O devices share the same address space as main memory, allowing the CPU to access them like memory locations.
 - Memory-mapped I/O eliminates the need for device drivers.
 - Memory-mapped I/O is only used for input devices, not output devices.
20. Which ONE of the following statements correctly explains programmed I/O and interrupt-driven I/O?
- In programmed I/O, the device notifies the CPU when it is ready, while interrupt-driven I/O requires continuous polling.
 - Programmed I/O allows the CPU to perform other tasks while waiting for the device to become ready.
 - Interrupt-driven I/O allows the CPU to perform other tasks and respond only when the device signals that it is ready.
 - Both programmed I/O and interrupt-driven I/O eliminate CPU involvement in data transfer completely.

Section B

Question 01 (20 Marks)

- a. Discuss the concept of process starvation in CPU scheduling. Explain how aging can be used to prevent starvation and identify which scheduling algorithms are suitable to mitigate this problem. (06 marks)
- b. A system has the following set of processes, each with its arrival time, burst time, and priority (lower number = higher priority). All timings are in milliseconds. (14 marks)

Table Q1: Process Timing Recorded Table

Process	Arrival Time (ms)	Burst Time (ms)	Priority
P1	0	8	3
P2	1	4	1
P3	2	9	4
P4	3	5	2
P5	4	2	5

Draw Gantt charts and calculate the average waiting time and average turnaround time for each of the following scheduling algorithms

- I. Shortest Job Next (Non-preemptive)
- II. Round Robin with a time-quantum of 3ms.

*Show all steps clearly.

Question 02 (20 Marks)

- a. List the four necessary conditions that must be held simultaneously for a deadlock to occur. For each condition, briefly describe one technique to eliminate it. (06 marks)
- b. The following sequence of events occurred (Table Q2) when allocating multiple resources to perform a function of a processor. "P" indicates a process and "R" indicates a resource. Answer all the sub questions according to the following sequence of events. (14 marks)
- i. Draw resource allocation graphs to analyze the above scenario using Holt's modeling method.
 - ii. Are there any deadlocked processes? If yes, name them. If not, indicate which events occurring next would cause a deadlock situation in the system.

Table Q2: Resources Distribution among Processes

Event	Action
1	P1 requests and gets R1
2	P2 requests and gets R3
3	P3 requests and gets R2
4	P1 requests and gets R2
5	P2 requests R1
6	P3 requests R3
7	P4 requests and gets R4
8	P1 requests R3
9	P4 requests R2
10	P3 requests R4

Question 03 (20 Marks)

- a. Discuss the relevance and validity of Moore's Law in the context of modern computing systems. (03 marks)
- b. Define following terms: (02 marks)
 - I. Clock Cycle Time
 - II. Throughput
- c. Assume that you have been running an important program on your company's 300MHz Pro1 processor. By running a detailed simulator, you were able to collect the following instruction mix and breakdown of costs for each instruction type (Table Q3): (15 marks)

Table Q4: Instruction Mix and their Breakdown of cost

Instruction Class	Frequency (%)	Cycles
Integer arithmetic and logical	40	1
Load	20	1
Store	10	2
Branches	20	3
Floating Point	10	5

* You must clearly show all intermediate steps in your calculations and state all formulas used.

- I. What is the CPI and MIPS rating of the Pro1 for this program?
- II. Suppose that you turn on the optimizer and it eliminates 30% of the arithmetic/logic instructions, 30% of load instructions, and 20% of the floating-point instructions. None of the other instructions are effected. What is the speedup of the optimized program?

- III. What is the CPI and MIPS rating with the optimized version of the program? Compare your result with above (c. I) and explain the difference.
- IV. Now, suppose that the Pro2 has just been introduced with a faster clock rate (450 MHz). However, in order to make the execution faster, the engineers had to increase the CPI for arithmetic, logical, and load instructions to 2 cycles and floating point instructions to 6 cycles. What is the speedup of the Pro2 over the Pro1 on the *unoptimized* program?

Question 04 (20 Marks)

- a. Define volatile and non-volatile memories and explain how both types of memory are utilized within the hierarchical memory system of a computer. (03 marks)
- b. Briefly explain the following terms related to cache memory (08 marks)
- I. Address Mapping
 - II. Replacement Policy
 - III. Store Policy
 - IV. Block Size
- c. A hierarchical memory system that uses cache memory has cache access time of 50 nano seconds, main memory access time of 300 nano seconds, 75% of memory requests are for read, hit ration of 0.8 for read access and the write-through scheme is used. What will be the average access time of the system both for read and write requests? (06 marks)
- Assume ~~cache~~ access time is not included in main memory access time. *cache*
- d. A hard disk has 128 sectors per track with 512 bytes per sector. The rotation rate is 5200 RPM. What is the transfer rate in bytes per second? (03 marks)

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Use this **sheet** to provide answers to the **Section A** (MCQ questions) and attach to the end of the answer script (booklet).

Mark "X" on the correct answer number.

Index No. :

EEX5563/ EEX5564 Final Examination 2024-25: Answers for **Section A**

Question Number	Answer			
1	a	b	c	d
2	a	b	c	d
3	a	b	c	d
4	a	b	c	d
5	a	b	c	d
6	a	b	c	d
7	a	b	c	d
8	a	b	c	d
9	a	b	c	d
10	a	b	c	d
11	a	b	c	d
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14	a	b	c	d
15	a	b	c	d
16	a	b	c	d
17	a	b	c	d
18	a	b	c	d
19	a	b	c	d
20	a	b	c	d