

THE OPEN UNIVERSITY OF SRI LANKA
B.SC. (IT) DEGREE PROGRAMME – 2026/2027
FINAL EXAMINATION
COU4304 – COMPUTER ARCHITECTURE
DURATION: TWO HOURS ONLY (2 HOURS)



Date: 20.06.2026

Time: 9.30 am - 11.30 am

INSTRUCTIONS TO CANDIDATES

Duration of the examination is **two (02) hours**.

This paper contains **six (06) questions** and **five (05) pages**.

The students should answer **any four (04) Questions Only**.

All the questions carry equal marks.

Write your **index number** clearly on the **cover of the answer book** and on **all extra sheets used**.

Clearly indicate the **question numbers** you are attempting in your answer script.

Begin each answer on a **new page**.

All answers **must be written in English**.

Do not use red pens. Only **blue or black pens** are allowed for writing answers.

Tie all additional sheets securely to your main answer script before handing it in.

This is a closed-book examination. No reference materials, textbooks, or electronic devices are allowed.

Candidates are reminded to maintain **academic integrity**. Any form of **cheating or misconduct** will result in **disciplinary action**.

Answer **FOUR** Questions **ONLY**.

Question 01

- a) What are the two (02) key functions performed by the Quick Path Interconnect (QPI) Link Layer? Briefly explain them. [05 marks]
- b) The Von Neumann model is the foundation of modern computer design. Describe the four (04) main structural components of the Von Neumann computer and explain the function of each. [06 marks]
- c) Explain the Von Neumann bottleneck. Your answer should address:
 - i. What causes the bottleneck?
 - ii. Why it limits performance?
 - iii. Two (02) architectural solutions used in modern systems. [08 marks]
- d) The Computer Level Hierarchy defines Six (06) levels of abstraction. Briefly describe following levels, clearly indicating the relationship between adjacent levels.
 - i. Digital Logic Level
 - ii. Microarchitecture (Control) Level
 - iii. Assembly Language Level [06 marks]

Question 02

- b) Explain what is meant by Register Transfer Level (RTL) design and state the three (03) main components that must be defined when representing a digital system at the RTL level. [05 marks]
- c) For each RTL statement below, state the operation being performed and explain its effect:
 - i. $R2 \leftarrow \text{shr } R3$
 - ii. $R4 \leftarrow R4 + 1$
 - iii. $T3 : (R1 \leftarrow R2, R2 \leftarrow R1)$ [06 marks]
- d) Describe the fetch-decode-execute-interrupt cycle of a processor. For each stage, state what operation is performed and which registers are involved. [06 marks]
- e) Describe the following stages of the CAD-based digital logic design flow, stating the purpose of each stage.
 - i. Synthesis
 - ii. Functional Simulation
 - iii. Timing Simulation
 - iv. Chip Configuration [08 marks]

Question 03

- a) Write short notes on the following topics.
- i. Cloud Computing
 - ii. Embedded systems [05 marks]
- b) Define Instruction Set Architecture (ISA) and explain its role as the interface between hardware and software. List four (04) types of information defined by an ISA. [06 marks]
- c) Differentiate between Moore and Mealy state machines with respect to output dependency and timing of output changes. [05 marks]
- d) A Finite State Machine (FSM) is used to model a simple traffic light controller with three (03) states: Green (S0), Yellow (S1), and Red (S2). Answer the following:
- i. Draw a clearly labelled state transition diagram for this traffic light FSM.
 - ii. Identify whether this FSM would be modelled as a Moore machine or a Mealy machine, and justify your answer.
 - iii. State two (02) differences between Moore and Mealy machines. [09 marks]

Question 04

- a) Define the term 'Virtual Memory' and state why it is used. [04 marks]
- b) Explain the three (03) different types of mapping techniques used in cache organization. [06 marks]
- c) RAID is widely used in enterprise storage systems.
- i. What does RAID stand for, and what are its two main goals?
 - ii. Compare RAID 0, RAID 1, and RAID 5 in terms of their striping/mirroring strategy, redundancy, and relative performance. [07 marks]
- d) The CPU execution time of a program can be expressed using the following relationship:

$$\text{CPU Time} = \text{Instruction Count} \times \text{CPI} \times \text{Clock Cycle Time}$$

Using this formula, answer the following:

- i. A program executes 2×10^8 instructions on a processor with a clock rate of 400 MHz and an average CPI of 2.0. Calculate the CPU execution time.
- ii. A second processor runs the same program with a clock rate of 600 MHz but requires an average CPI of 3.5. Calculate the CPU execution time for this processor.
- iii. Which processor gives better performance? Show your calculation and express the performance ratio. [08 marks]

Question 05

- a) The registers in the processor perform two (2) roles. Briefly explain them. [03 marks]
- b) Briefly describe following terms.
- Job Scheduler
 - Medium Term Scheduler
 - Paging
- [06 marks]
- c) Identify and describe states A, B, C and D in the given process state model diagram.

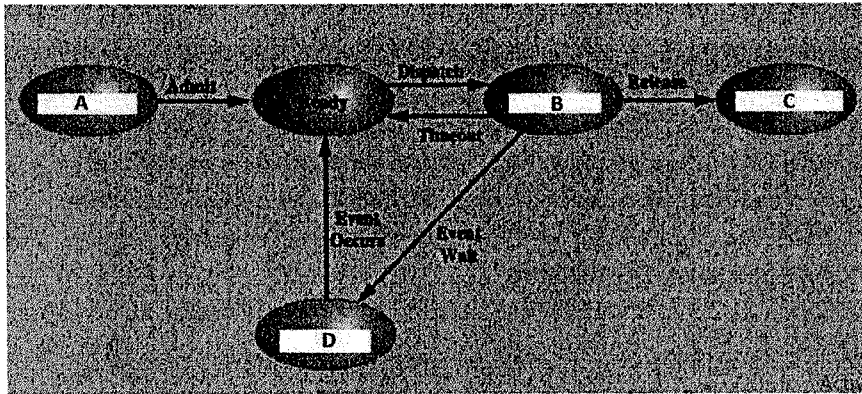


Figure: Process state model diagram

[08 marks]

- d) Consider the logic function: $f = (x_1 \cdot x_3) + (\bar{x}_3 \cdot x_2)$
 Write the Verilog implementation of this function using:
- Structural representation (gate-level primitives)
 - Behavioural representation (continuous assignment using assign)
- Clearly identify the module name, port declarations, and signal names in both implementations. [08 marks]

Question 06

- a) Define the following computer performance metrics and state the unit of measurement for each:
- Response Time
 - Throughput
 - CPU Execution Time
- [03 marks]
- b) Machine A completes a benchmark program in 10 seconds. Machine B completes the same program in 20 seconds.
- Calculate the performance of each machine
 - How many times faster is Machine A than Machine B?
- [06 marks]

- c) A computer engineering lab is evaluating a processor used in an embedded system. The processor operates with a clock cycle time of 4 nanoseconds. A benchmark program is executed on this system, and its performance is analyzed.
- Calculate the clock frequency of the processor in MHz.
 - If the benchmark program requires 5×10^8 clock cycles to complete, calculate the total CPU execution time. [05 marks]
- d) A network router receives packets at a rate of 20 packets per second. Each packet remains in the system for an average of 0.25 seconds.
- Using Little's law, calculate the average number of packets in the router.
 - If the arrival rate doubles, determine the new average number of packets, assuming the time spent remains unchanged. [06 marks]
- e) A program has 70% of its execution time that can be parallelized. The parallelizable portion is improved by a factor of 4.
- State Amdahl's Law.
 - Calculate the overall speedup of the program. [05 marks]

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