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THE OPEN UNIVERSITY OF SRI LANKA
BACHELOR OF SOFTWARE ENGINEERING - LEVEL 5
ECX5263 - COMPUTER ORGANIZATION AND OPERATING SYSTEMS
FINAL EXAMINATION 2011
DURATION : THREE HOURS

DATE : 18th March 2012 **TIME : 1400 - 1700 HOURS**

Answer any *five* questions. All questions carry equal marks.

1.

(i) Add the following numbers as fixed-point integers. Your calculations must be shown by using binary numbers in two's complement. Choose appropriate word length.

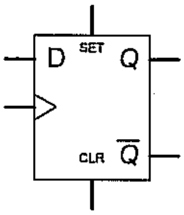
(a) -20.5 + 0.25

(b) 9.625 + 0.75

(ii) Represent all the above numbers as floating point numbers of the following format using biased exponent.

S (1 bit)	Exponent (8-bit)	Mantissa (23-bit)

(iii) Draw a truth table for a typical *D Flip-flop* given in the following figure. Using the same *D Flip-flop* draw a schematic diagram for an 8-bit register.



2.

(i) Draw the complete *process state transition* diagram and describe it for a typical multi-user operating system.

(ii) Draw typical virtual machine schematics for different styles of Instruction Set Architecture (ISA) i.e. Accumulator, Memory-Memory, Stack, Load-Store.

(iii) Identify the general purpose and special purpose registers in each of the architectures mentioned above.

(iv) Write a program using the ISA (given in the Appendix) of the Accumulator architecture of the Students' Experimental Processor (SEP) to find the elements of the array *X* according to the following formula:

$X_i = (A_i + B_i)/2$; where $i = 1$ to n.

Assume that all elements of the arrays and the value *n* are stored in the memory.

3. An enhancement in a computer system improves only some part of the system. Accordingly improvement of the performance depends on the impact of the enhanced part. The f denotes the fraction of the computation time in the old system that can be improved with the enhancement made; S_e is the achievable speedup only if the enhanced part of the system is used.

   (i) If the old time of the system (without improvement) is T_{old} formulate the new time T_{new} of the system after the enhancement.

   (ii) The speedup of the new system (after the improvement) is

   $$S_{new} = \frac{T_{old}}{T_{new}}.$$

   Accordingly derive the Amdahl's law in terms of f, S_e, S_{new}.

   (iii) Restate this law for multiprocessor system, where f is the fraction of the computation time which is parallelizable, n is the number of processors in the system.

   (iv) Initially multiprocessor system has 8 processors. To improve the system it is decided to double the number of processors. What would be the minimum fraction of parallelizable part of an application that increases the speedup by more than 1.7 times of the old system?

4.

   (i) Describe why operating systems need Process Control Box (PCB).

   (ii) Describe what the pre-emptive and non pre-emptive algorithms are. Give 2 examples for each of them.

   (iii) Given the following information:

Job #	**Arrival Time**	**CPU Time**
1	0	7
2	1	2
3	2	2
4	2	1
5	4	3

   Draw a time line for each of the following scheduling algorithms and compute the waiting time and turnaround time for every job.

   (a) First Come First Served

   (b) Round Robin (using a time quantum of 1, ignore context switching and natural wait)

5.

   (i) What is meant by a page fault in virtual memory organization?

   (ii) When a page fault occurs describe what the computer system would do.

   (iii) A disk subsystem employed for the virtual memory organization has the following specifications: 32 sectors per track, 512 bytes per sector, 3600 rpm, average linear latency of 30 ms, page size of 4 Kbytes. In average the computer system executes an instruction in 1.5 μs.

   (a) Calculate the data transfer rate of the disk subsystem.

(b) Compute the wasted time in the event of a page fault while executing a program.

(c) What should be the seek time of the disk drive in order to reduce the wasted time, to less than 85%?

6.

(i) Throughput of a pipeline is inversely proportional to the bottleneck of the pipeline. Explain the statement.

(ii) An instruction execution path will take 9ns to execute an instruction in one-stage pipeline. However this logic path can be divided into any number of stages and the logic delay (9ns) can be subdivided equally as well. Moreover the sum of setup time of a latch and clock skew will be 1ns. Let *s* as the number of stages. Assume that the pipeline receives a set of instructions without branching instructions.

(a) What is the clock period T_{clock} in terms of *s*?

(b) What is the execution time of 101 instructions?

(c) Calculate the optimum number of stages that the pipeline should have for minimum execution time of 101 instructions.

7.

(i) There are 2 types of memory management schemes: Static (Fixed) partition memory allocation and Dynamic (Variable) partition memory allocation. Compare these schemes with their advantages and disadvantages when allocating memory. Draw diagrams where necessary.

(ii) Explain how you prevent the occurrence of a deadlock.

(iii) Draw a Resource Allocation Graph for the following.

There are 3 Processes (P1, P2, and P3) and 4 different types of Resources (R1, R2, R3, and R4). Instances for each resource are 1, 1, 2, and 3 respectively.

- P1 requests an instance of R1 and is holding an instance of R3.
- P2 requests an instance of R3 and is holding one instance of R1 and one instance of R2.
- P3 requests an instance of R3 and R2, and is holding an instance of R4.

(a) Is there any chance to occur a deadlock? Show how it could happen.

(b) Propose a method to avoid the deadlock at the current situation.

8.

(i) Name three organizations of cache memory and describe them briefly.

(ii) Briefly describe design options of a cache using Sets, Sectors, Block Slots, and Allocation Units (AUs).

(iii) While sophisticated file managers implement file sharing by allowing several users to access a single copy of a file at the same time, others implement file sharing by providing copy of the file to each user. List the advantages and disadvantages of each method.

(iv) Compare and contrast dynamic memory allocation and the allocation of files in secondary storage.

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Appendix

ISA of Accumulator Architecture

Arithmetic instructions		
ADD	Addition	Acc ← Acc + op
SUB	Subtraction	Acc ← Acc - op
MUL	Signed multiplication	Acc (16 bit) ← Acc(8 LSBs) * op(8 LSBs)
DIV	Unsigned division	Acc ← Acc / op2
INC	Increment by 1	Acc ← Acc + 1
Logical instructions		
AND	Bit-wise And	Acc ← Acc AND op
OR	Bit-wise OR	Acc ← Acc OR op
XOR	Bit-wise XOR	Acc ← Acc XOR op
SHL	Shift left by 1-bit	CF ← Acc (MSB), op← Acc (14 down to 0) & 0
SHR	Shift right by 1-bit	CF ← Acc (LSB), Acc ← 0 & Acc (15 down to 1)
ROL	rotate left by 1-bit	CF ← Acc (MSB), op← Acc (14 down to 0) & CF
ROR	rotate right by 1-bit	CF ← Acc (LSB), Acc ← CF & Acc (15 down to 1)
NOT	One's compliment negation	op1 ← NOT Acc
Control Transfer instructions		
Conditional Branches		
JC	Jump if carry	If CF =1 then IP ← IP + Operand
JOF	Jump if over-flow	If OF =1 then IP ← IP + Operand
JS	Jump if Sign	If SF =1 then IP ← IP + Operand
JP	Jump if parity	If PF =1 then IP ← IP + Operand
JZ	Jump if result is zero	If ZF =1 then IP ← IP + Operand
Unconditional branch		
JUMP	Jump	IP ← IP + Operand
Loops		

LOOZ	Loop until zero	Count ← Count – 1
		IF Count =0; Loop termination
		ELSE; IP ← IP + operand

Calls and Returns		
CALL	Procedure call	implied return address ← IP IP ← Immediate address
RETURN	Return from procedure	IP ← Contents of implied return address
Miscellaneous instructions		
NOP	No operation	
Data Movement instructions		
LOADacc	Copy the operand to the accumulator	Immediate: Acc ← op Direct: Acc ← memory (op)
STOREacc	Copies the accumulator to the memory address	Direct: Memory (op) ← Acc Indirect : Memory {memory (op)} ← Acc