THE OPEN UNIVERSITY OF SRI LANKA
BACHELOR OF SOFTWARE ENGINEERING - LEVEL 5
ECX5263 COMPUTER ORGANIZATION AND OPERATING SYSTEMS
FINAL EXAMINATION 2013
DURATION : THREE HOURS

DATE : 31st August 2014 **TIME : 0930 - 1230 HOURS**

Answer any ***five*** questions. All questions carry equal marks.

1.

(i) Add the following numbers as fixed-point integers. Your calculations must be shown by using binary numbers in two's complement. Choose appropriate word length.

(a) -11.5 + (-1.75)

(b) -12.125 + 2.25

(ii) Represent all the above numbers as floating point numbers of the following format using biased exponent.

S (1 bit)	Exponent (7-bit)	Mantissa (24-bit)

(iii) In a source code a programmer declared an array of floating point numbers. All elements of the array are in the above format given in the question 1.(ii). Your task is to hide a text in English using this array and all characters of the text are in extended ASCII codes (8 bits). A floating point number represents only one character and the character is written in Most Significant Bits of the respective floating point number.

(a) Show that after hiding a text in English the array contains only positive numbers and the numbers are always greater than 1.

(b) What will be decimal numbers of the array if you hide the text OUSL? The ASCII code of the each letter is 79, 85, 83 and 76 in decimal respectively.

2.

(i) Comment on the following statement giving reasons.

"MIPS rating does not accurately represent the performance of a computer."

(ii) If processor A has a higher clock rate than processor B, and processor A also has a higher MIPS rating than processor B, explain whether processor A will always execute faster than processor B.

(iii) Suppose that there are two implementations of the same instruction set architecture. Machine A has a clock cycle time of 20ns and an effective CPI of 1.5 for some program, and machine B has a clock cycle time of 15ns and an effective CPI of 1.0 for the same program. Which machine is faster for this program and by how much?

3.

(i) Draw typical virtual machine schematic for Stack Architecture and briefly describe the functionality of it.

(ii) Compare and contrast Stack architecture with Accumulator architecture considering performance, size of the processor and size of the code of a program.

(iii) Write a program using the ISA (given in the Appendix) of the Accumulator architecture of the Students' Experimental Processor (SEP) to find the total (X) of all positive values of an array, i.e.

$$X = \sum_{i=1}^{n} A_i \text{ ; where } A_i > 0.$$

Assume that all elements of the array and the value n are stored in the memory.

4.

(i) Describe the term *deadlock* in computer systems.

(ii) What are the main objectives of a resource manager?

(iii) Draw a Resource Allocation Graph for the following.

There are 3 Processes (P1, P2, and P3) and 3 different types of Resources (R1, R2 and R3). Instances for each resource are 2, 1 and 1 respectively.

- P1 requests an instance of R2 and is holding an instance of R1.
- P2 requests an instance of R1 and R3.
- P3 requests an instance of R1 and R3, and is holding an instance of R2.

(a) Is there any chance to occur a deadlock if non-pre-emptive scheduler is used? Show how it could happen.

(b) Propose a method to avoid the deadlock at the current situation.

5.

(i) What are the advantages and disadvantages when using a single bus as a shared communication link between memory, processor and I/O devices?

(ii) Compare hard disk drives with solid state drives considering cost, performance, capacity and reliability.

(iii) A disk drive has eight surfaces, with 512 tracks per surface and a constant 64 sectors per track. Sector size is 1 Kbytes. The average seek time is 8ms, the track-to-track access time is 1.5ms, and the drive runs at 3600 rpm. Successive tracks in a cylinder can be read without head movement.

(a) What is the drive capacity?

(b) What is the average access time for the drive?

(c) Estimate the time required to transfer a 5-MB file.

(d) What is the burst transfer rate?

6.

(i) Name three organizations of cache memory and describe them briefly.

(ii) Why are the first level caches usually split (instructions and data are in different caches) while the L2 is usually unified (instructions and data are both in the same cache)?

(iii) For a data cache with a 92% hit rate and a 2-cycle hit latency, calculate the average memory access latency. Assume that latency to memory and the cache miss penalty together is 124 cycles. Note: The cache must be accessed after memory returns the data.

7.

(i) Describe how state transition diagram is useful in any process description.

(ii) Describe the technique called Context Switching in operating systems.

(iii) Consider spending your holiday at a resort with your friends. You will travel to the resort for a week. There you will spend your time engaging in different activities such as playing games, relaxing, enjoying food, reading books and so on. There are no time specific activities other than the schedule time for breakfast, lunch and dinner.

(a) Draw a state transition diagram for spending your holiday at the resort.

(b) What information you have to save in the Process Control Block in the process of spending your holiday.

8.

(i) Describe what the pre-emptive and non pre-emptive algorithms are. Give two examples for each of them.

(ii) Name four scheduling algorithms. Describe two of them briefly.

(iii) How do you compute the waiting time and turnaround time for a process in a computer system? Give examples for the calculations.

(iv) Consider a machine with 32-bit virtual addresses, 32-bit physical addresses, and a 4KB page size. Consider a two-level page table system where each table occupies one full page. Assume each page table entry is 32 bits long. To map the full virtual address space, how much memory will be used by the page tables?

Appendix

ISA of Accumulator Architecture

Arithmetic instructions		
ADD	Addition	Acc ← Acc + op
SUB	Subtraction	Acc ← Acc - op
MUL	Signed multiplication	Acc (16 bit) ← Acc(8 LSBs) * op(8 LSBs)
DIV	Unsigned division	Acc ← Acc / op2
INC	Increment by 1	Acc ← Acc + 1
Logical instructions		
AND	Bit-wise And	Acc ← Acc AND op
OR	Bit-wise OR	Acc ← Acc OR op
XOR	Bit-wise XOR	Acc ← Acc XOR op
SHL	Shift left by 1-bit	CF ← Acc (MSB), op← Acc (14 down to 0) & 0
SHR	Shift right by 1-bit	CF ← Acc (LSB), Acc ← 0 & Acc (15 down to 1)
ROL	rotate left by 1-bit	CF ← Acc (MSB), op← Acc (14 down to 0) & CF
ROR	rotate right by 1-bit	CF ← Acc (LSB), Acc ← CF & Acc (15 down to 1)
NOT	One's compliment negation	op1 ← NOT Acc
Control Transfer instructions		
Conditional Branches		
JC	Jump if carry	If CF =1 then IP ← IP + Operand
JOF	Jump if over-flow	If OF =1 then IP ← IP + Operand
JS	Jump if Sign	If SF =1 then IP ← IP + Operand
JP	Jump if parity	If PF =1 then IP ← IP + Operand
JZ	Jump if result is zero	If ZF =1 then IP ← IP + Operand
Unconditional branch		
JUMP	Jump	IP ← IP + Operand
Loops		
LOOZ	Loop until zero	Count ← Count – 1 IF Count =0; Loop termination ELSE; IP ← IP + operand
Calls and Returns		
CALL	Procedure call	implied return address ← IP IP ← Immediate address
RETURN	Return from procedure	IP ← Contents of implied return address
Miscellaneous instructions		
NOP	No operation	
Data Movement instructions		
LOADacc	Copy the operand to the accumulator	Immediate: Acc ← op Direct: Acc ← memory (op)
STOREacc	Copies the accumulator to the memory address	Direct: Memory (op) ← Acc Indirect : Memory {memory (op)} ← Acc