The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination –2005
ECU 4309 – Electronic Systems Engineering **(Closed Book)**

Time: 0930-1230hrs. Date: 04.05.2006

Answer any five questions.

1. Consider the current mirror circuit shown in Figure-Q1.

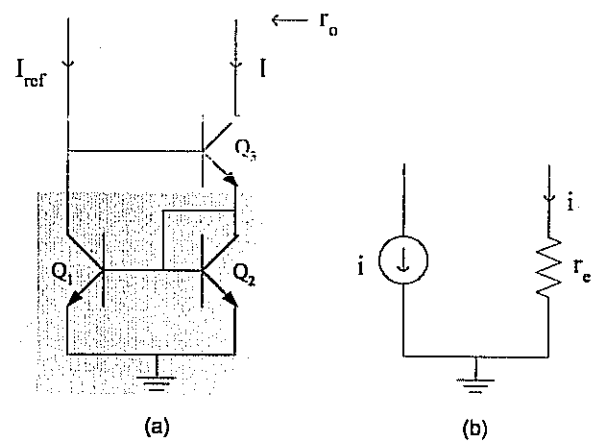

Figure-Q1

(a) If the three transistors are matched, show that the current I in Figure-Q1(a) is given by

$$I_{ref}\frac{1}{1+\frac{2}{\beta(2+\beta)}}$$

(b) Show that the small signal equivalent circuit of the shaded block can be approximated to the circuit in Figure-Q1(b), where r_e is given by $\frac{h_{ie}}{h_{fe}}$. Neglect h_{re} and h_{oe} of Q_1 and Q_2.

(c) Using the result obtained in (b), draw the small signal equivalent circuit for Figure-Q1(a) taking into account h_{oe} of Q_3. Hence show that the output resistance r_0 is given by $\frac{h_{fe}}{2h_{oe}}$. You may neglect h_{re} of Q_3. State clearly any other assumptions.

2. A differential amplifier is shown in Figure-Q2, in which TR_1 and TR_2 are matched. The current gain β is 100 for all transistors in the circuit. Assume that the transistors are at the room temperature.

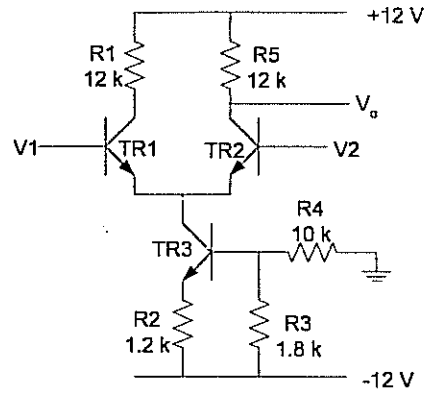

Figure-Q2

(a) Find the maximum swing of the output.

(b) Show that the output voltage V_o is given by $\frac{12}{1+e^{-40V_D}}$ where $V_D = V_1 - V_2$.

(c) Using the result obtained in (b), derive the small signal differential voltage gain when $V_1 = V_2$.

(d) Calculate CMRR if the Early voltage of TR_3 is 100V. You may neglect the output resistance of TR_1 and TR_2. The output resistance of a transistor is given by $\frac{V_E}{I_C}$, where V_E is the Early voltage and I_C is the collector current.

3. The circuit shown in Figure-Q3 uses two ideal operational amplifiers.

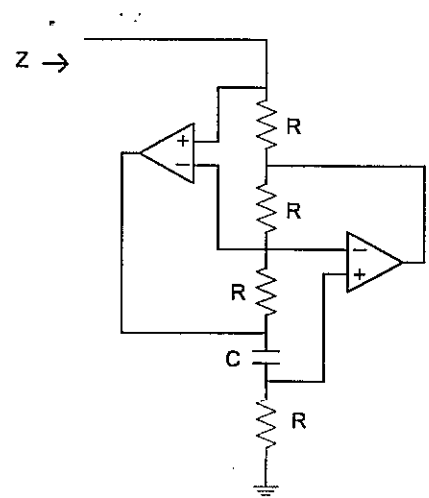

Figure-Q3

(a) Derive the impedance Z looking in to the direction of the arrow shown in the Figure-Q3. What can you say about the function of this circuit?

(b) Use this circuit to design a second order high pass filter with cut off frequency 100kHz and quality factor 7. Assume that the impedance of the driving source is 50Ω and the filter output is connected to a large resistance. All capacitors used in your design must be equal in value.

4. A four step R-2R ladder circuit is shown in Figure-Q4(a).

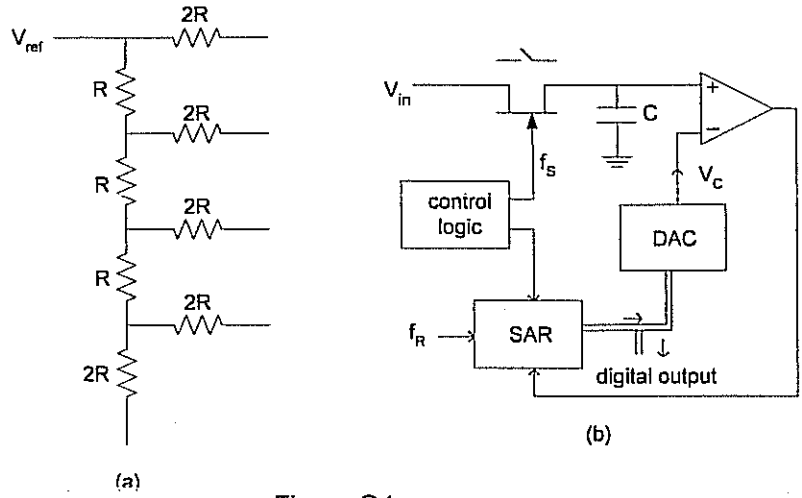

Figure-Q4

(a) Show how this circuit can be used to form a 4-bit digital to analog converter to give a minimum output of $-\frac{15}{16}V_{ref}$.

(b) An analog to digital converter based on successive approximation technique is shown in Figure-Q4(b). The digital output is in the signed 8-bit 2^S complement form in the range –128 to +127. The value of LSB of the converter is 0.1V.

(i) What is the digital output for an input voltage of –7.72V? Show the conversion sequence by tabulating the digital output and the DAC output voltage against the clock pulses for this input.

(ii) Assume that the sampling switch takes 60ns to close and the propagation delays of the SAR, DAC and the comparator are 150ns, 100ns and 50ns respectively. Calculate the minimum conversion time taken to convert an input voltage. Estimate the maximum frequency of the sampling clock f_S and the SAR clock f_R. You may neglect the propagation delay in the control logic and assume that the output of SAR is set properly before starting a conversion.

(iii) Calculate the minimum value of C in order to have capacitor voltage droop(reduction in the capacitor voltage) within $\pm\frac{1}{2}LSB$ during a conversion. The input bias current of the comparator is 3μA.

5. (a) An amplifier can be represented with a finite gain A and a dominant pole at ω_o. When this amplifier is provided with negative feedback, show that the effective bandwidth can be increased by $(1+A\beta)$, where β is the feedback factor.

(b) Consider the circuit shown in Figure-Q5.

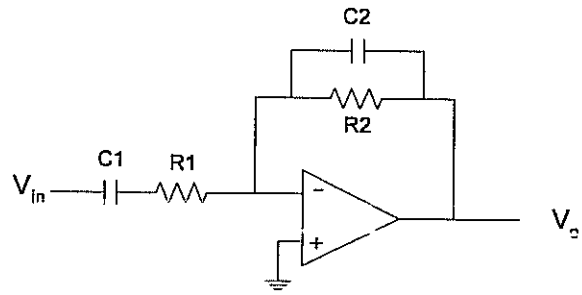

Figure-Q5

(i) Assuming that the amplifier is an ideal op-amp, derive the voltage transfer function and identify the poles and zeros.

(ii) Sketch the Bode magnitude and phase plots with labeled axes. Assume $R_2C_2 < R_1C_1$.

(iii) Select values of components C_1 and C_2 for this circuit to differentiate input signals below $100\,Hz$ and to integrate signals above $100\,kHz$, if $R_1 = 3.3k\Omega$ and $R_2 = 100k\Omega$. Show how you can minimize the error at the output due to the input bias current.

6. An amplifier to be used for high frequency signals is shown in Figure-Q6. The driving source resistance is 75Ω and the external load at the output is 300Ω.

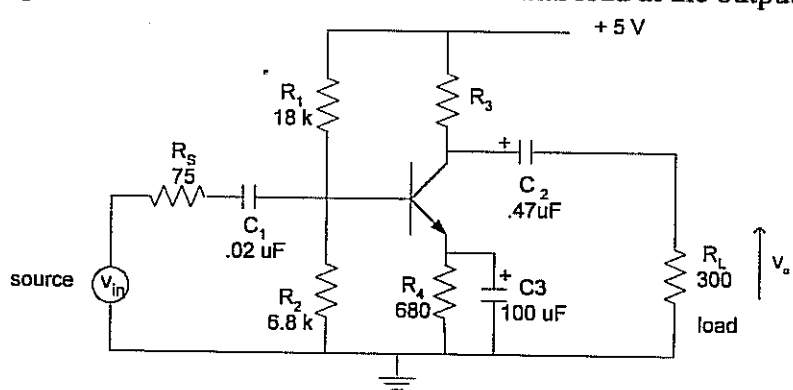

Figure - Q6

(a) Determine the value of R_3 in order to have a voltage gain of -10 throughout the bandwidth.

(b) Derive the two-pole transfer function of the circuit at high frequencies and find the pole frequencies. Hence determine the upper bandwidth limit. Use the following device data.

$r_{bb'} = 50\Omega \qquad r_{b'e} = 2k\Omega \qquad g_m = 40\times10^{-3}\,\frac{A}{V} \qquad C_{b'e} = 0.65pF$

$C_{b'c} = 0.55pF$

Assume the values of $r_{b'c}$ and r_{ce} to be infinite.

7. (a) One method of implementing combinational logic is using multiplexers. Draw the block diagram of an 8-input multiplexer. Implement the following logic function using an 8-input multiplexer.

$$F = \Sigma\, 0,1,4,6,8,9,10,14,15$$

(b) Design a logic circuit based on a finite state machine to detect the string of digits 1011 in a serial binary data stream using a minimum number of D flip-flops and logic gates. Assume that the data and the clock lines are available, where the data is synchronized with the clock. Show the state diagram, state table and the steps of your design clearly.

8. (a) With the aid of diagrams show how static-1 and static-0 hazards are generated in a logic circuit.

(b) Find all static hazards in the circuit shown in Figure-Q8. Show the transitions of the inputs that will generate these hazards.

(c) Implement the logic function ensuring hazard free operation. You must show that all hazards are removed in the implementation.

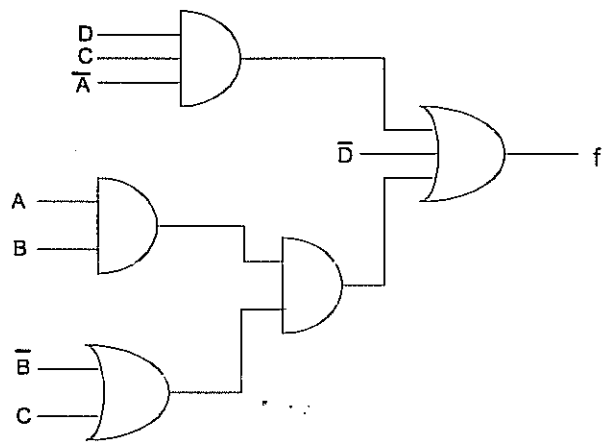

Figure-Q8