THE OPEN UNIVERSITY OF SRI LANKA
BACHELOR OF TECHNOLOGY - LEVEL 5
ECX5236 – COMPUTER ARCHITECTURE
FINAL EXAMINATION 2005

DURATION : THREE HOURS

062

DATE : 19th April 2006 **TIME : 0930 - 1230 HOURS**

Answer any ***five*** questions. All questions carry equal marks.

1.
(i) Briefly describe the tasks of an I/O system of a computer.
(ii) Briefly describe the following I/O control systems: Programmed I/O, Interrupt I/O, and Coprocessor I/O.
(iii) A processor executes instructions at a rate of M MIPS. An I/O subroutine for writing data to a disk requires I number of instructions. The disk has a total latency of t_l seconds. A program, executing on the processor, writes its data on the disk N number of times at different occasions. The program takes T seconds to complete its execution.
(a) Derive an equation to calculate the efficiency of the system if it uses only the programmed I/O.
(b) Analyzing the equation derived show what hardware and software changes can be done to improve the efficiency.

2.
(i) Explain the Amdahl's law and derive an equation for that.
(ii) The MIPS rating of a processor is 1000. However the processor requires at least one memory access per instruction. The memory latency of the system is 10 ns.
(a) What is the MIPS rating of the system.
(b) Performance of the system depends very much on the memory. Propose three solutions for this performance problem. Describe them briefly.
(c) If you are able to double the MIPS rating of the processor what is the achievable overall speedup of the system. Assume that there is no change in memory latency. Solve the problem using the Amdahl's law.

3. A design of an instruction execution path has L logic delays. So it will take L time to execute an instruction in one-stage pipeline. However the logic path can be divided into a number of stages. In the multistage pipeline it is assumed that logic delay L is equally subdivided. Accordingly in each stage the minimum clock period is calculated as $T_{clock} = t_{\max} + \tau$; where t_{max} is approximated to the largest delay of a stage and τ is the sum of setup time of a latch and clock skew. Let k as the length of the instruction sequence and s as the number of stages.
(a) What is the clock period T_{clock} in terms of L, s and τ?
(b) What is the execution time of the k number of instructions?
(c) Derive an equation to calculate the optimum number of stages in the pipeline.

(d) Prove that minimum execution time of k number of instructions is $\left(\sqrt{L}+\sqrt{\tau(k-1)}\right)^2$

4.

(i) Describe the two methods, namely hardwired and microprogrammed control, in designing the Control Unit of a computer.

(ii) The hardwired control design of a Control Unit can be accomplished in 5 steps. Briefly explain those steps.

(iii) Describe and distinguish between vertical microinstructions and horizontal microinstructions.

(iv) In order to evaluate the cost of each design, microprogrammed or the hardwired control we can use the chip area required for each design. In a particular design microprogramming has a fixed cost of 1000 units of chip area and a variable cost of 1 unit of chip area for the ROM to store each microinstruction. Hardwired control has a cost of 5 units of chip for each instruction. When will the microprogrammed control method be more economical?

5. You are to connect an external device to a computer through a parallel port. The device accepts a data byte when its *Accept data* pin receives a rising edge of a signal. Immediately the device will set its *data valid* pin to low. As soon as the data byte is written to its memory the *data valid* pin will set to high. The device accepts data only when the *data valid* pin is high.

(i) Draw a block diagram to show the connectivity of the device with the computer. Indicate which pins of the parallel port you are going to connect with the pins of the device.

(ii) Draw a typical timing diagram for data transferring from the computer to the device.

(iii) Give an algorithm for sending a byte to the device from the computer through the parallel port. You must show all addresses of the relevant ports and values of the ports each time when they are used.

(iv) Expand your algorithm to send a file to the device.

6.

(i) Briefly describe the major objectives of a memory hierarchy.

(ii) Describe the working principle of cache memory.

(iii) Comment on the following statement giving reasons.

"Hit ratio can be improved by using faster memory i.e. memory with less access time."

(iv) A virtual memory system has memory access time of 500 ns, secondary storage access time of 20ms and average access time of 4.4ms.

(a) Compute the hit ratio for the virtual memory system.
(b) Describe two suitable hardware and/or software schemes to reduce the average access time.

7.

(i) Briefly describe the Memory-Memory and Load-Store architectures. What are the major differences in those architectures?

(ii) You are asked to design a simple CPU with the following specifications. Only 256 Kbytes of address space are needed. In order to make the CPU as simple as possible it has been restricted to 16 instructions with 2 different addressing modes. You have the option of deciding the number of registers in the CPU.

(a) How many registers would you suggest for the design? Explain.
(b) Draw a suitable instruction format for your design.
(c) What addressing modes do you select for instructions? Give reasons for your selection.
(d) Draw a complete architecture of your design. You have to show the data path and the memory interfaced with the CPU.

8.

(i) Briefly describe Very Long Instruction Word (VLIW) approach of Multiple-issue processors.

(ii) What are the advantages and disadvantages of a Superscalar implementation and a VLIW approach?

(iii) Compare single component and multi component addressing modes.

(iv) What are the addressing modes of the following Intel 8086 instructions?

(a) MOV AL, BL ; (AL) ← (BL)
(b) ADD AL, data ; (AL) ← (AL) + data
(c) AND AX, addr ; (AX) ← (AX) AND (addr)

Note : *AL, AX* and *BL* belong to the register set. Here *addr* is an address of a memory location and *data* is a data value.

Appendix

Parallel port connector description

Pin: D-sub	Signal	Function	Source	Register		Inverted at con-nector?	Pin: Centron-ics
				Name	Bit #		
1	nStrobe	Strobe D0-D7	PC[1]	Control	0	Y	1
2	D0	Data Bit 0	PC[2]	Data	0	N	2
3	D1	Data Bit 1	PC[2]	Data	1	N	3
4	D2	Data Bit 2	PC[2]	Data	2	N	4
5	D3	Data Bit 3	PC[2]	Data	3	N	5
6	D4	Data Bit 4	PC[2]	Data	4	N	6
7	D5	Data Bit 5	PC[2]	Data	5	N	7
8	D6	Data Bit 6	PC[2]	Data	6	N	8
9	D7	Data Bit 7	PC[2]	Data	7	N	9
10	nAck	Acknowledge (may trigger interrupt)	Printer	Status	6	N	10
11	Busy	Printer busy	Printer	Status	7	Y	11
12	PaperEnd	Paper end, empty (out of paper)	Printer	Status	5	N	12
13	Select	Printer selected (on line)	Printer	Status	4	N	13
14	nAutoLF	Generate automatic line feeds after carriage returns	PC[1]	Control	1	Y	14
15	nError (nFault)	Error	Printer	Status	3	N	32
16	nInit	Initialize printer (Reset)	PC[1]	Control	2	N	31
17	nSelectIn	Select printer (Place on line)	PC[1]	Control	3	Y	36
18	Gnd	Ground return for nStrobe, D0					19,20
19	Gnd	Ground return for D1, D2					21,22
20	Gnd	Ground return for D3, D4					23,24
21	Gnd	Ground return for D5, D6					25,26
22	Gnd	Ground return for D7, nAck					27,28
23	Gnd	Ground return for nSelectIn					33
24	Gnd	Ground return for Busy					29
25	Gnd	Ground return for nInit					30
	Chassis	Chassis ground					17
	NC	No connection					15,18,34
	NC	Signal ground					16
	NC	+5V	Printer				35

[1]Setting this bit high allows it to be used as an input (SPP only)

[2]Some Data ports are bidirectional.

Parallel port register definitions

Base address: 0378h

Data Register (Base Address)

Bit	*Pin: D-sub*	Signal Name	Source	Inverted at connector?	Pin: Centroni
0	2	Data bit 0	PC	no	2
1	3	Data bit 1	PC	no	3
2	4	Data bit 2	PC	no	4
3	5	Data bit 3	PC	no	5
4	6	Data bit 4	PC	no	6
5	7	Data bit 5	PC	no	7
6	8	Data bit 6	PC	no	8
7	9	Data bit 7	PC	no	9

Some Data ports are bidirectional. (See Control register, bit 5 below.)

Status Register (Base Address +1)

Bit	*Pin: D-sub*	Signal Name	Source	Inverted at connector?	Pin: Centroni
3	15	nError (nFault)	Peripheral	no	32
4	13	Select	Peripheral	no	13
5	12	PaperEnd	Peripheral	no	12
6	10	nAck	Peripheral	no	10
7	11	Busy	Peripheral	yes	11

Additional bits not available at the connector:
0: may indicate timeout (1=timeout).
1, 2: unused

Control Register (Base Address +2)

Bit	*Pin: D-sub*	Signal Name	Source	Inverted at connector?	Pin: Centroni
0	1	nStrobe	PC[1]	yes	1
1	14	nAutoLF	PC[1]	yes	14
2	16	nInit	PC[1]	no	31
3	17	nSelectIn	PC[1]	yes	36

[1]When high, PC can read external input (SPP only).
Additional bits not available at the connector:
4: Interrupt enable. 1=IRQs pass from *nAck* to system's interrupt controller. 0=IRQs do not pass to interrupt controller.
5: Direction control for bidirectional Data ports. 0=outputs enabled. 1=outputs disabled; Data port can read external logic voltages.
6,7: unused