THE OPEN UNIVERSITY OF SRI LANKA
BACHELOR OF TECHNOLOGY - LEVEL 5
ECU 3303 – COMPUTER SYSTEMS ARCHITECTURE
FINAL EXAMINATION 2005

DURATION : THREE HOURS

038

DATE : 19th April 2006 TIME : 0930 - 1230 HOURS

Answer any ***five*** questions. All questions carry equal marks.

1.
(i) Briefly describe the tasks of an I/O system of a computer.
(ii) Briefly describe the following I/O control systems: Programmed I/O, Interrupt I/O, and Coprocessor I/O.
(iii) For the virtual memory organization a hard disk is purchased for employing disk subsystem. According to the vendor the following specifications are given: 8 GB capacity, 1024 cylinders, 255 heads, 63 sectors, 7200 rpm and average seek time 9 ms. The page size of the virtual memory is 8 Kbytes. Performance of the computer system is given as 100 MIPS

(a) Calculate the number of bytes in a sector of the hard disk. (Note: bytes in a sector should be the nearest to the power of two value)
(b) Calculate the data transfer rate of the disk subsystem.
(c) Compute the wasted time in the event of a page fault while executing a program.
(d) What should be the seek time of the disk drive in order to reduce the wasted time, to be less than 85%?

2. An enhancement in a computer system improves only some part of the system. Accordingly improvement of the performance depends on the impact of the enhanced part. The f denotes the fraction of the computation time in the old system that can be improved with the enhancement made; S_e is the achievable speedup only if the enhanced part of the system is used.
(i) If the old time of the system (without improvement) is T_{old} formulate the new time T_{new} of the system after the enhancement.
(ii) The speedup of the new system (after the improvement) is

$$S_{new} = \frac{T_{old}}{T_{new}}.$$

Accordingly derive the Amdahl's law in terms of f, S_e, S_{new}.
(iii) Restate this law for multiprocessor system, where f is the fraction of the computation time which is parallelizable, n is the number of processors in the system.
(iv) Initially multiprocessor system has 8 processors. To improve the system it is decided to double the number of processors. What would be the minimum fraction of parallelizable part of an application that increases the speedup by more than 1.7 times of the old system?

3.
(i) Prove that maximum achievable speedup of a linear pipeline is equal to its number of stages.
(ii) A soft drink bottling factory has three independent functional machines to fill the bottle with soft drink, to seal the bottle and to label it. Each machine takes 2 seconds to complete its own task of filling, sealing and labelling. Working order of the above

tasks are; first filling then sealing and finally labelling. If the pipeline concept is used in this scenario, what will be the total time to complete the tasks of filling, sealing and labelling of 1000 bottles, which are being kept in the queue.

(iii) If the above mentioned 3 independent machines takes 3, 4, and 2 seconds per bottle to complete its own task of filling, sealing and labelling respectively; what will be the speedup that can be gained when using pipeline technique?

4.

(i) Only the following two constraints are valid for the processes A, B, C, D and E.

$\overline{A}\underline{A}\overline{B}\underline{B}\overline{C}\underline{C}\overline{D}\underline{D}\overline{E}\underline{E}$

$\overline{B}\underline{B}\overline{C}\underline{C}\overline{A}\underline{A}\overline{D}\underline{D}\overline{E}\underline{E}$

where $\overline{X}$ - initiation of the process,

$\underline{X}$ - termination of the process.

(a) Show how the processes A, B, C, D and E can be organised in parallel.

(b) State a situation where this parallelism is not possible.

(ii) In the following computation, a, b, and c are three external inputs and z is the final output.

$$z = \frac{a+b+c+a*b+b*c+a*c}{a*b*c}$$

where * denotes multiplication.

Give a precedence graph for the solution considering parallelism as much as possible. State clearly tasks of each process in the graph. You are free to use any number of intermediate results.

5.

(i) What does Redundant Array of Inexpensive Disks (RAID) mean?

(ii) Two computers are connected each other through their COM2 serial ports. These ports are operating at 9600bps and are based on 8250 family UARTs.

(a) Give a flowchart of a subroutine that transmits an ASCII character (7 bits) using odd parity, 1 start bit, and 2 stop bits. Clearly state all values of port registers and their addresses wherever they are used. For necessary port register description refer to the appendix.

(b) Show how you use the above subroutine to send a file (all character codes are less than 127) to the other computer.

(c) Estimate the minimum transmission time if the file is n Kbytes in size.

6.

(i) Briefly describe the major objectives of a memory hierarchy.

(ii) Describe the working principle of cache memory.

(iii) Comment on the following statement giving reasons.

"Hit ratio can be improved by using faster memory i.e. memory with less access time."

(iv) A virtual memory system has memory access time of 500 ns, secondary storage access time of 20ms and average access time of 4.4ms.

(a) Compute the hit ratio for the virtual memory system.

(b) Describe two suitable hardware and/or software schemes to reduce the average access time.

7.

(i) Briefly describe the Memory-Memory and Load-Store architectures. What are the major differences in those architectures?

(ii) You are asked to design a simple CPU with the following specifications. Only 256 Kbytes of address space are needed. In order to make the CPU as simple as possible it has been restricted to 16 instructions with 2 different addressing modes. You have the option of deciding the number of registers in the CPU.

(a) How many registers would you suggest for the design? Explain.
(b) Draw a suitable instruction format for your design.
(c) What addressing modes do you select for instructions? Give reasons for your selection.
(d) Draw a complete architecture of your design. You have to show the data path and the memory interfaced with the CPU.

8.

(i) Briefly describe Very Long Instruction Word (VLIW) approach of Multiple-issue processors.

(ii) What are the advantages and disadvantages of a Superscalar implementation and a VLIW approach?

(iii) Compare single component and multi component addressing modes.

(iv) What are the addressing modes of the following Intel 8086 instructions?

(a) MOV AL, BL ; (AL) ← (BL)
(b) ADD AL, data ; (AL) ← (AL) + data
(c) AND AX, addr ; (AX) ← (AX) AND (addr)

Note : *AL, AX* and *BL* belong to the register set. Here *addr* is an address of a memory location and *data* is a data value.

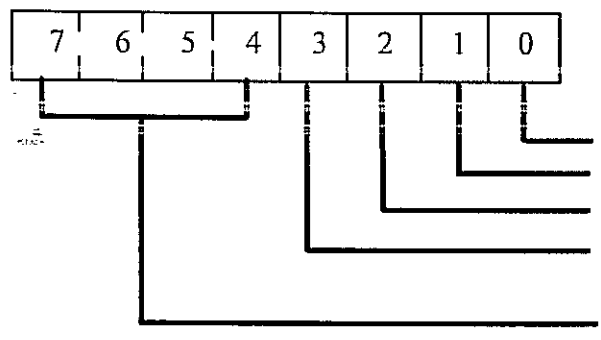
Appendix

8250 Family Register Definitions

Register Name	Offset	Abbreviation	Access Type
Receiver Buffer Register	0	RBR	Read Only
Transmit Holding Register	0	THR	Write Only
Interrupt Enable Register	1	IER	Read/Write
Interrupt Identification Register	2	IIR	Read Only
FIFO Control Register (16550)	2	FCR	Write Only
Line Control Register	3	LCR	Read/Write
Modem Control Register	4	MCR	Read/Write
Line Status Register	5	LSR	Read Only
Modem Status Register	6	MSR	Read Only
Divisor Latch (16 bits)	0/1	DL	Read/Write

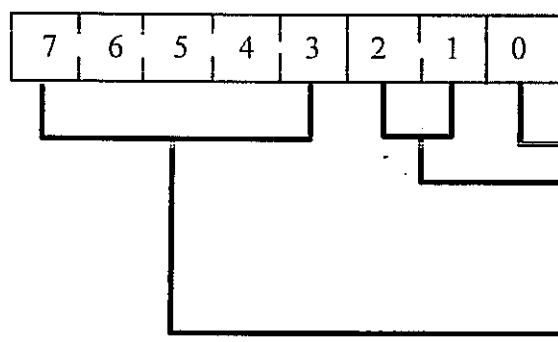
Base address of COM1 - 3F8h Base address of COM2 - 2F8h

IER



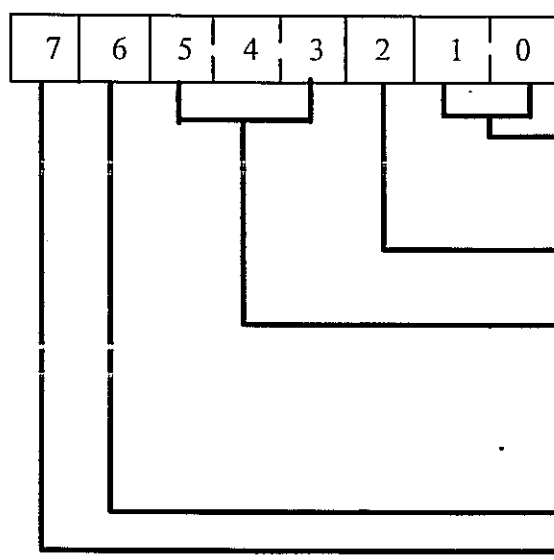
1- Received Data Available
1- Transmit Holding Register Empty
1 - Line Status
1 - Modem status (CTS, DSR, DCD or RI changes state)
Not used (= 0)

IIR



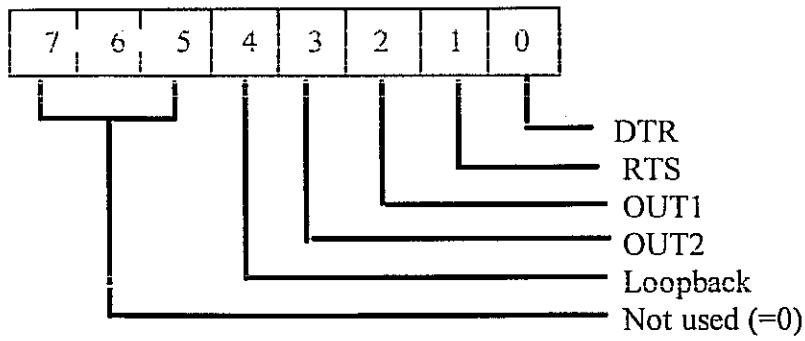
1 - No interrupt Rending
00 - Modem Status Interrupt
01 - Transmit Holding Register Empty
10 - Received Data Available
11 - Line Status
Not used (= 0)

LCR

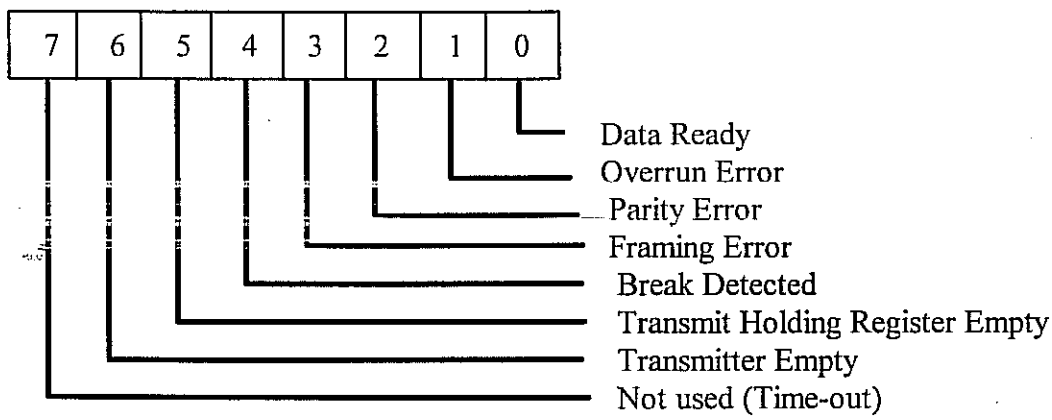


Word length Select
00 - 5 bits 10 - 7 bits
01 - 6 bits 11 - 8 bits
Number of Stop Bits
0 - 1 bit 1 - 2 bits
Control Bits
000 - No parity 100 - No Parity
001 - Odd Parity 101 - Mark Parity
010 - No Parity 110 - No Parity
011 - Even Parity 111 - Space Parity
Break Control
Divisor Latch Access Bit
1- Divisor Latch
0 - as usual RBR/ THR and IER

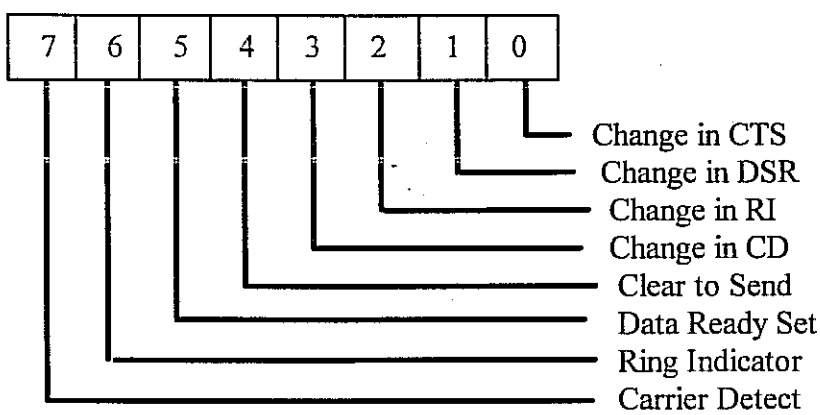
MCR


7
6
5
4
3
2
1
0
DTR
RTS
OUT1
OUT2
Loopback
Not used (=0)

LSR


7
6
5
4
3
2
1
0
Data Ready
Overrun Error
Parity Error
Framing Error
Break Detected
Transmit Holding Register Empty
Transmitter Empty
Not used (Time-out)

MSR


7
6
5
4
3
2
1
0
Change in CTS
Change in DSR
Change in RI
Change in CD
Clear to Send
Data Ready Set
Ring Indicator
Carrier Detect