The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination –2006
ECX 5330 – Electronic Systems

108

(Closed Book)

Date: 22.03.2007 Time: 0930-1230 hrs.

Answer any five questions.

1. (a) The op-amp shown in Figure-Q1 has a finite gain A_0, infinite input impedance and zero output impedance. Write an expression for the closed loop voltage gain. Give the value of feed back factor and the loop gain. What is the closed loop gain if the amplifier is ideal?

   (b) Calculate the minimum open loop gain that will give a closed loop gain within 1% from the gain value of the ideal case.

   (c) If the op-amp has a dominant pole with the open loop gain of 5×10^3 and a gain-bandwidth product of 5×10^4Hz, derive an expression for its closed loop gain and sketch the magnitude and phase Bode plots. Label the axes and mark important values in your sketch.

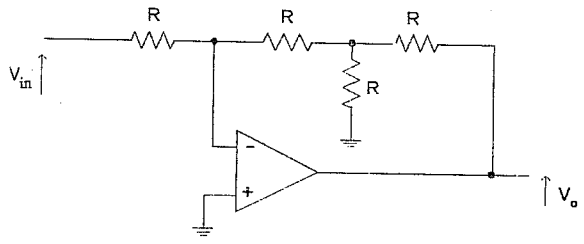

Figure - Q1

2. In the circuit shown in Figure-Q2(a), the op-amp is ideal and the transistors are matched.

   (a) Find V_0 in terms of I_{C1} and I_{C2}.

   (b) Using Ebers-Moll relationship, derive an expression for the transconductance $\frac{\partial(I_{C1} - I_{C2})}{\partial(V_1 - V_2)}$ in terms of V_1 and V_2 and evaluate its value for $V_1 = V_2$. Hence derive V_0 in terms of V_1 and V_3, if $V_2 = 0$. What are the limitations for V_1 and V_2 for proper operation?

   (c) Determine the function of the circuits shown in Figure-Q2(b) and Figure-Q2(c), if the block P shown in them uses the circuit in Figure-Q2(a). Also indicate the useful range of the input signals.

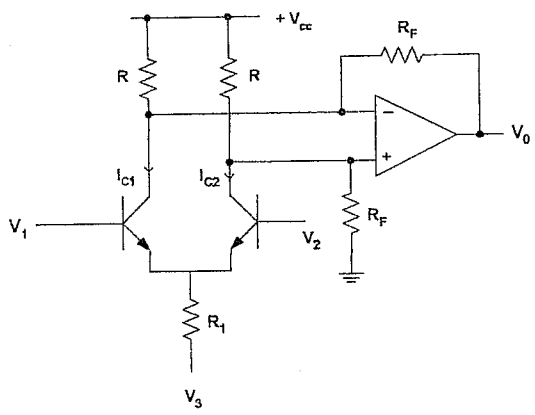

FIGURE - Q2(a)

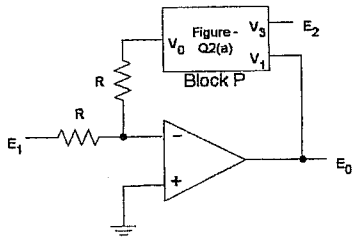

FIGURE - Q2(b)

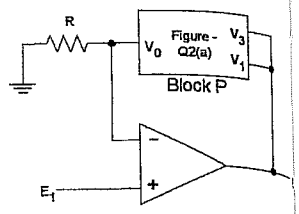

FIGURE - Q2(c)

3. (a) Show that the circuit in Figure-Q3(a) is a logarithmic amplifier. State the main disadvantage of this circuit and its effects on the amplifier characteristics.

(b) Derive the output V_0 of the circuit shown in Figure-Q3(b) in terms of V_1 and V_2. Hence suggest a use of this circuit. Compare the stability of the characteristics of this circuit with (a) above. You may assume that all transistors are of the same type but not matched. State why it is useful to have R_4 Adjustable.

(c) The op-amps A_1, A_2 and A_3 each has an input offset voltage of 10mV and an input bias current of 40nA. Find the percentage error of the output voltage if $V_1 = 40$mV and $V_2 = 20$ mV. Neglect the offset voltage and the input bias current of A_4. Assume $R_1 = R_3 = 10$K.

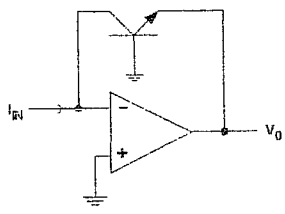

FIGURE - Q3(a)

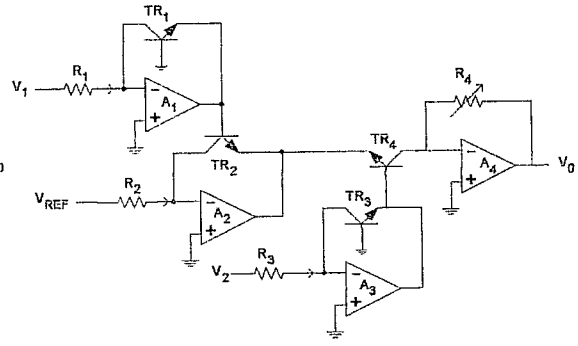

FIGURE - Q3(b)

4 (a) Explain what is meant by 'dominant pole compensation' and by 'lag-lead compensation' with respect to amplifiers. Show how you are going to introduce the poles and zeros in each case.

(b) An op-amp has a voltage gain of 10^6 with two poles at 10^4 Hz and 10^8 Hz.

(i) What is the bandwidth of the amplifier? Write the open loop gain function $H(\omega)$.

(ii) Sketch the gain and phase Bode plots with labeled axes.

(iii) Find the range of usable closed loop gain to have a phase margin not less than 45^0. What is the maximum possible bandwidth, the closed loop gain and the feedback factor under this condition?

(iv) It is required to use this amplifier with a feedback factor of 0.1 while having a phase margin of 45^0 using lag-lead compensation.

Find the position of the poles and zeros to be introduced and give the values of the compensation network components. The value of any capacitor used should not exceed 0.1μF.

5. (a) State how Miller's effect can modify the input capacitance of a common drain amplifier and a common source amplifier.

(b) Draw the high frequency equivalent circuit of the MOSFET amplifier shown in Figure-Q5.

(c) Derive the two pole solution for the voltage gain at high frequencies. Neglect r_d of the MOSFET.

(d) Determine the mid-band gain and the high frequency 3dB cutoff point.
$g_m = 2mA/V$ $c_{gs} = 3pF$ $c_{gd} = 3pF$ $c_{ds} = 1pF$

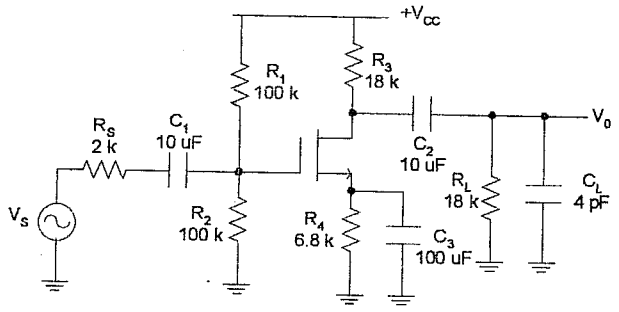

Figure - Q5

6. The circuit shown in Figure-Q6 is a section of a dual slope integrating analog to digital converter. Assume the op-amp and the comparator is ideal. The functions p(t), q(t), m(t), u(t) and z(t) are voltages at the positions shown.

(a) If m(t) is a constant, derive $\frac{du}{dt}$ in terms of q(t) and m(t).

(b) The switch is in position A for a time T and then changed to position B until the comparator output is changed and then turned to position C. If the time elapsed in position B is t, derive an expression for p(t) in terms of T, t and m(t). Assume that u(t) is zero initially and the signals p(t) and m(t) are constant during the process.

(c) If p(t) = 4V, m(t) = -6V, R = 27k and C = 1μF, draw the waveforms of q(t), u(t) and z(t) on a common time scale showing the time and voltage values. Assume the switch is in position C and u(t) is zero initially. The time T is 24 ms.

(d) If a control signal for time t is available, show in a block diagram how you can obtain a digital output corresponding to the input p(t) and justify your answer.

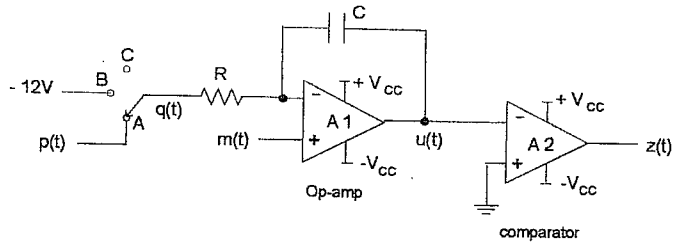

Figure - Q6

7. A Sallen-Key low pass filter circuit is shown in Figure-Q7.

(a) Derive the transfer function from the first principles.

(b) Find component values for a Butterworth filter having a cut-off frequency of 200 kHz.

(c) Using the results obtained in (b), give the circuit diagram with component values of a Butterworth high pass filter having a cut-off frequency of 200kHz.

(d) Show how you can apply the concepts used in (b) and (c) to have a band-pass filter scheme having a bandwidth of 100kHz – 200kHz and give the circuit diagram with component values.

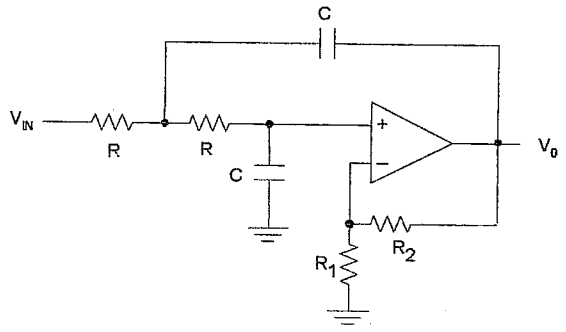

Figure - Q7

8. An implementation of a synchronous finite state machine is shown in Figure-Q8. It has two inputs X and Y, one output Z and two state variables A and B. The state assignment for the four states S_0, S_1, S_2 and S_3 are as follows.

S_0 : A = 0, B = 0 S_2 : A = 1, B = 0

S_1 : A = 0, B = 1 S_3 : A = 1, B = 1

(a) Derive the input equations of the flip-flops and the output equation.

(b) Write the state equations.

(c) Derive the state transition table.

(d) Draw the state diagram for the state machine.

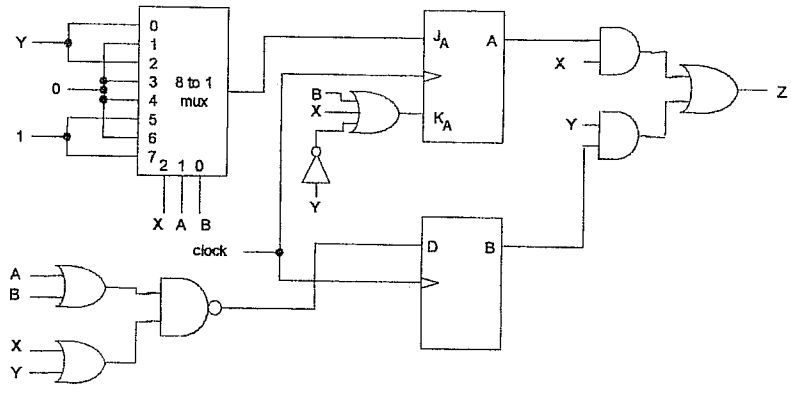

FIGURE - Q8