The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination –2007
ECX 5330 – Electronic Systems **(Closed Book)**

Time: 0930-1230hrs. Date: 13.05.2008

Answer any five questions.

1. A differential amplifier is shown in Figure-Q1, in which TR1 and TR2 are a matched pair. The current gain β is 100 for the three transistors. Assume that the transistors are at the room temperature and $V_T = 0.025\,V$.

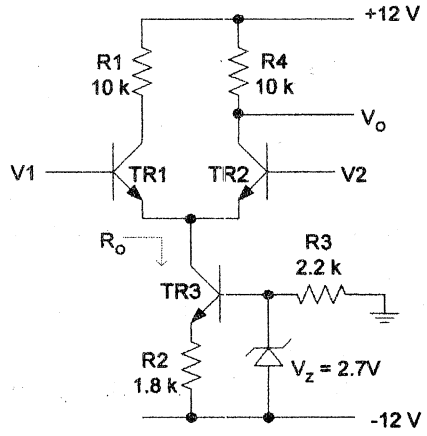

Figure-Q1

(a) The differential input voltage V_D is given by $V_D = V_1 - V_2$. Show that the small signal differential voltage gain $\frac{v_O}{v_D}$ is given by $\frac{462e^{40V_D}}{\left(1+e^{40V_D}\right)^2}$. Hence calculate its value for $V_1 = V_2$. You may neglect the output resistance of the three transistors.

(b) Show the resistance R_O for ac signals is given by $r_{ce}\left[1+\frac{g_m R_2}{\frac{R_2}{r_{be}}+1}\right]$ where r_{ce}, r_{be} and g_m are of TR3. Assume $R_2 << r_{ce}$.

(c) Calculate CMRR for this circuit. You may neglect the output resistance of TR1 and TR2. Use the following data for TR3.
$g_m = 100\,mA/V$ $r_{be} = 1K$ Early voltage = 50V

2. Consider the current mirror circuit shown in Figure-Q2.

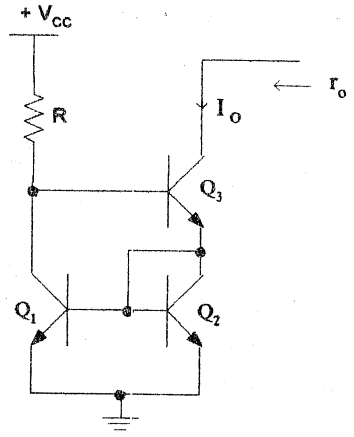

Figure-Q2

(a) If the three transistors are matched, show that the current I_o is given by $\dfrac{(V_{CC}-2V_{BE})}{R\left(1+\dfrac{2}{\beta(\beta+2)}\right)}$.

(b) Find out the minimum value of β for I_o to be within 0.99 of the 'reference current' of the current mirror.

(c) Determine the value of R so that $I_o = 80\mu A$, $V_{cc} = 5V$ and $\beta = 100$. State any other assumptions if necessary.

(d) Show that the output resistance r_o of the circuit is given by $r_{ce}\left(1+\dfrac{g_m^2 r_{be}}{2\left(g_m+\dfrac{1}{r_{be}}\right)}\right)$ if $r_{ce} >> 1$. Neglect r_{ce} of Q_1 and Q_2.

3. (a) The collector signal current i_c of a bipolar transistor class A amplifier with a resistive load is given by, $i_c = K_1 i_b + K_2 i_b^2$; where i_b is the base current. If i_b is a sinusoidal variation, show that the percentage 2nd harmonic distortion in i_c is given by $50\dfrac{(I_{max}+I_{min}-2I_Q)}{(I_{max}-I_{min})}$; where I_Q is the quiescent collector current, I_{max} and I_{min} are the maximum and minimum values of the collector current respectively.

(b) A class A transistor power amplifier operating with a 60V power supply has a resistive load of 16Ω. The amplifier is biased to have a quiescent collector current of 2.1A. With a sinusoidal input, the collector voltage varies between 9V and 51V. Calculate the percentage 2nd harmonic current distortion, power output at the fundamental frequency and the conversion efficiency based on useful output.

4. (a) Show that if an amplifier is provided with negative feedback, its performance is close to ideal when $A\beta >> 1$; where β is the feedback factor and A is the open loop gain.

(b) The operational amplifier used in Figure-Q4 has a finite gain A and can be considered as ideal in all other respects.

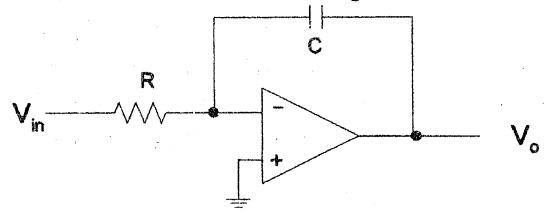

Figure-Q4

(i) Derive the voltage gain transfer function of this circuit.

(ii) Sketch the magnitude and phase Bode plots of the voltage gain. On the same diagram sketch the magnitude and the phase plots if the op-amp is ideal.

(iii) If the op-amp is a real dominant pole amplifier having a low frequency gain of 60dB and a pole at 100Hz, determine the frequency range for which this circuit can be used as an integrator. Assume $R = 1.59k$ and $C = 0.01\mu F$. Show your steps clearly.

5. (a) State how Miller's effect can modify the input capacitance of a common collector amplifier and a common emitter amplifier.

(b) Draw the high frequency small signal equivalent circuit of the amplifier shown in Figure-Q5.

(c) Derive the two pole solution for the voltage gain $\frac{V_o}{V_{in}}$ at high frequencies.

You may neglect r_{ce} of the transistor.

(d) Determine the mid-band gain and the high frequency 3dB cutoff point.

$r_{bb'} = 100\,\Omega$ $r_{b'e} = 1k$ $C_{b'e} = 30\ pF$ $C_{cb} = 3\ pF$ $g_m = 50\ mA/V$

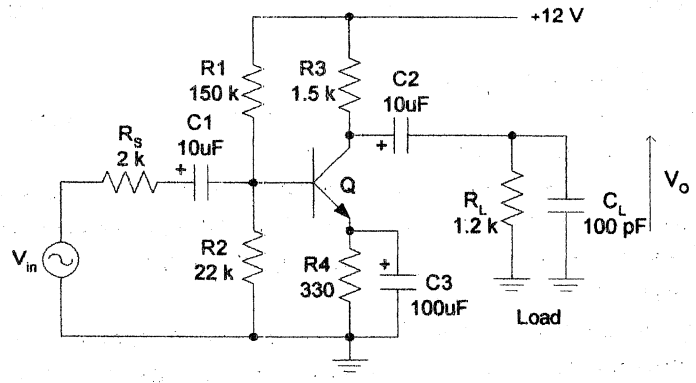

Figure-Q5

6. (a) Derive the transfer function of the circuit shown in Figure-Q6 in terms of A, Z_1, Z_2, Z_3 and Z_4.

(b) Select the type of components required for Z_1, Z_2, Z_3 and Z_4 in order to form a low pass filter. What is the order of the filter?

(c) A Butterworth low pass filter having a cut off frequency of 1KHz is to be implemented with this circuit using an operational amplifier. Draw a suitable circuit diagram and derive the values of the components. Show the frequency scaling and impedance scaling clearly.

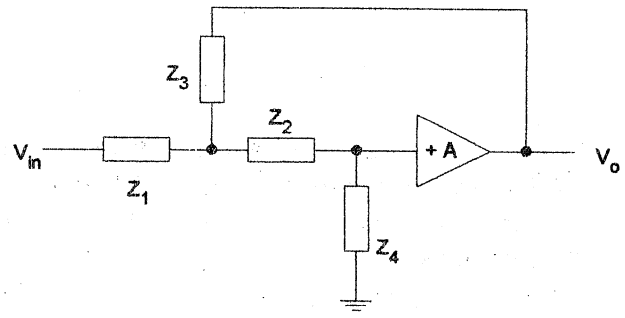

Figure-Q6

7. The two bit binary numbers A_1A_0 and B_1B_0 are the inputs to a two bit multiplier circuit.

(i) Derive the minimal expressions of the logic functions for *M, N, P* and *Q* which are the binary outputs of the multiplier, where *M* is the most significant bit and the order of the bits are *MNPQ*.

(ii) Implement *P* and *M* using two input NAND gates.

(iii) Implement *N* using a eight input multiplexer.

(iv) Implement *P* and *Q* using a four input, two output, eight product term Programmable Logic Array.

8. The state diagram of the Synchronous State Machine (SSM) shown in Figure-Q8(a) has a single input *X* and a single output *Y*. The states are represented by a two bit number *S*.

(a) Draw the transition table.

(b) If the next state is denoted by a two bit number S^+, derive Boolean expressions for *Y* and for each bit of S^+.

(c) If the SSM ends up in a unused state, find the next states for all input conditions. Observe the operation of the SSM based on your result.

(d) Implement the SSM using D-type flip-flops with the minimum number of logic gates.

(e) Complete the timing diagram shown in Figure-Q8(b) by indicating the state during each clock cycle and the waveform of Y. The circuit is initially in the state 'o' and active on the positive edge of the clock.

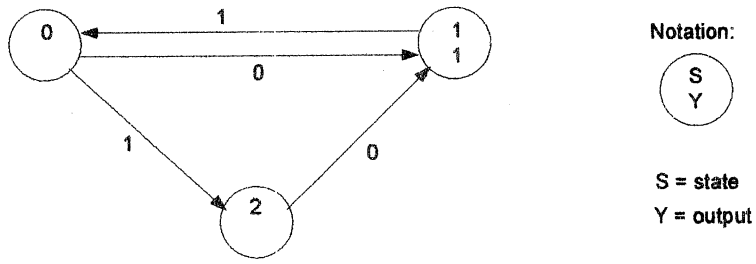

Figure-Q8(a)

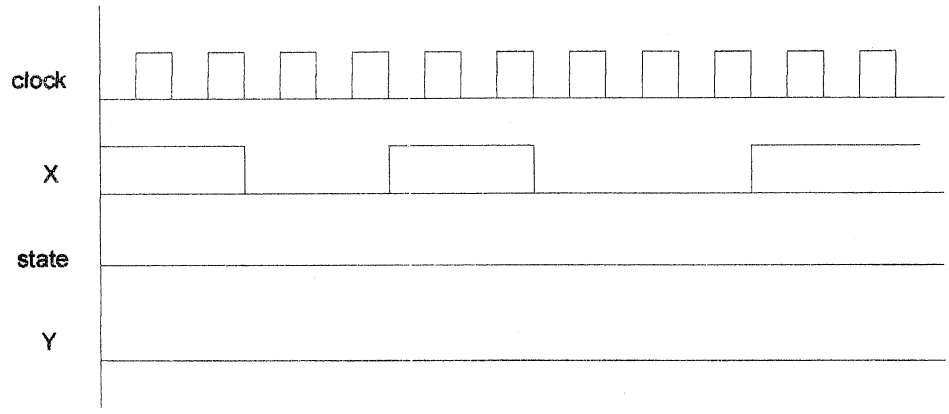

Figure-Q8(b)