THE OPEN UNIVERSITY OF SRI LANKA
BACHELOR OF TECHNOLOGY - LEVEL 5
ECX5236 – COMPUTER ARCHITECTURE
FINAL EXAMINATION 2007

DURATION : THREE HOURS

DATE: 14th May 2008 TIME: 0930 - 1230 HOURS

Answer any *five* questions. All questions carry equal marks.

1. A computer is constructed using a 3.6 GHz processor. It is integrated with 512 MB RAM which has 1.5 ns latency. The processor has 3 types of instructions: Branch, Arithmetic & Logic, and Memory move. The processor needs 5, 4, and 5 clocks to execute each type of instructions respectively. It is observed that of all the instructions executed 20% are branch instructions and 40% are Arithmetic and Logic operations. Branch and Memory Move instructions need 2 memory access but Arithmetic and Logic instructions need only one.

   (i) Calculate the average CPI of the processor.

   (ii) Find the MIPS rating of the processor

   (iii) Calculate the MIPS rating of the computer.

   (iv) Estimate the time taken to execute a program with n number of instructions.

2.

   (i) Briefly describe the addressing modes: Indirect, Immediate and Register.

   (ii) Consider $n \times m$ matrix. The matrix is stored in the memory. When a program needs an element (i, j) it has to use a suitable addressing mode to find the Effective Address of the element.

      (a) Propose an addressing mode for indexing a matrix. Describe it.

      (b) Show how it can be used for finding the Effective Address of an element of the matrix.

      (c) Provide a digital hardware design for calculating the Effective Address according to your proposed addressing mode.

3. Consider the process of the student registration of the Open University of Sri Lanka. First you have to collect the student file and then have to go to the student affairs desk to enter/ update student's personal data. Thereafter you must go to one of the academic counsellors (usually there are about 5 counsellors at the registration) at counsellor's desk for counselling and to offer courses for that academic year. After counselling you are directed to the file scrutinizing desk and then to the desk where the student record book is updated. Finally you collect your text books and finish the registration process. Normally there are about 200 students coming for registration and it takes about 6 hours to register all students in a day.

(i) Draw a block diagram suited for the expression of the complete process of student registration. (Hint: assume a task done by a person at any registration desk as one sub-task of the registration process.)

(ii) Analyzing the present process of student registration, name the technique used here to speed up the registration.

(iii) Estimate the maximum time taken to serve a student at any desk.

(iv) According to the system described above where is the bottleneck of the process of student registration? How it is solved here?

(v) What is the maximum speedup that can be gained in this process against the normal way of doing student registration i.e. all sub-tasks are done by one person?

4.

(i) Name three organizations of cache memory and describe them briefly.

(ii) Briefly describe design options of a cache using Sets, Sectors, Block Slots, and AUs.

(iii) Distinguish between Cache Addressing and Virtual Memory Page Addressing.

(iv) Derive a model for effective latency of a two-level cache. Assume L1 cache has a latency of 1 cycle. Transport time from L2 to L1 is T_{c21}, memory to L2 is T_{mc2}. H_1 and H_2 are the hit ratio of the L1 and L2 caches, respectively. Assume that all references are satisfied in one of the 3 memory levels.

5.

(i) Describe the two methods, namely hardwired and microprogrammed control, in designing the Control Unit of a computer.

(ii) The hardwired control design of a Control Unit can be accomplished in 5 steps. Briefly explain those steps.

(iii) Describe and distinguish between vertical microinstructions and horizontal microinstructions.

(iv) In order to evaluate the cost of each design, microprogrammed or the hardwired control we can use the chip area required for each design. In a particular design microprogramming has a fixed cost of 1000 units of chip area and a variable cost of 1 unit of chip area for the ROM to store each microinstruction. Hardwired control has a cost of 5 units of chip for each instruction. When will the microprogrammed control method be more economical?

6. You are to connect an external device, which sends sensor values as a 4 bit data to a computer through the parallel port or through the ISA bus. The device sets its *data valid* pin when it is ready to send data. As soon as the device receives *Data accepted* signal it resets *data valid* pin until the next data is ready.

(i) Draw a block diagram to show the connectivity of the device with the computer through the parallel port (Appendix A) or ISA bus (Appendix B). Indicate which pins of the parallel port or the ISA bus you are going to connect with the pins of the device.

(ii) Draw a typical timing diagram for reading data from the device.

(iii) Give an algorithm for receiving a 4 bit data from the device. You must show all values used for configuring the ISA bus (values for address bus and the data bus) or the parallel port (addresses and values of the relevant ports) each time when they are used.

(iv) Expand your algorithm to continuously receive data in a given period of time.

7.

(i) Briefly describe the advantages of Redundant Array of Inexpensive Disks (RAID).

(ii) Describe two methods of communication between two devices: synchronous and asynchronous.

(iii) Briefly describe the following I/O control systems: Programmed I/O, Interrupt I/O, and Coprocessor I/O.

(iv) A transaction processing system is considered for a PC. The PC executes instructions at 100 MIPS and has a disk with a total mean access time of 20 ms. Four disk accesses and 100,000 instructions are needed for each transaction. How many transactions per second are possible with this system?

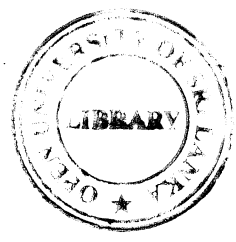
8.

(i) Describe the Flynn's classification (SISD, SIMD, MISD and MIMD) on computer organisation giving block diagrams for each organization.

(ii) A SIMD computer has 8 synchronized processor elements (PE) which are connected to each other via interconnection network. Each PE has a set of working registers and a data-routing register R to transfer and to receive data to and from other PEs.

(a) Design an algorithm for the SIMD computer to calculate the sum of an array (A) of 8 elements. Assume that element A_i is stored in the local memory of PE_i, where $i = 1, 2, 3 \ldots 8$.

(b) Briefly describe how the control unit of the SIMD computer controls the PEs according to your algorithm.



ndix A

Parallel port connector description

Signal	Function	Source	Register		Inverted at con-nector?	Pin: Centror -ics
			Name	Bit #		
nStrobe	Strobe D0-D7	PC[1]	Control	0	Y	1
D0	Data Bit 0	PC[2]	Data	0	N	2
D1	Data Bit 1	PC[2]	Data	1	N	3
D2	Data Bit 2	PC[2]	Data	2	N	4
D3	Data Bit 3	PC[2]	Data	3	N	5
D4	Data Bit 4	PC[2]	Data	4	N	6
D5	Data Bit 5	PC[2]	Data	5	N	7
D6	Data Bit 6	PC[2]	Data	6	N	8
D7	Data Bit 7	PC[2]	Data	7	N	9
nAck	Acknowledge (may trigger interrupt)	Printer	Status	6	N	10
Busy	Printer busy	Printer	Status	7	Y	11
PaperEnd	Paper end, empty (out of paper)	Printer	Status	5	N	12
Select	Printer selected (on line)	Printer	Status	4	N	13
nAutoLF	Generate automatic line feeds after carriage returns	PC[1]	Control	1	Y	14
nError (nFault)	Error	Printer	Status	3	N	32
nInit	Initialize printer (Reset)	PC[1]	Control	2	N	31
nSelectIn	Select printer (Place on line)	PC[1]	Control	3	Y	36
Gnd	Ground return for nStrobe, D0					19,20
Gnd	Ground return for D1, D2					21,22
Gnd	Ground return for D3, D4					23,24
Gnd	Ground return for D5, D6					25,26
Gnd	Ground return for D7, nAck					27,28
Gnd	Ground return for nSelectIn					33
Gnd	Ground return for Busy					29
Gnd	Ground return for nInit					30
Chassis	Chassis ground					17
NC	No connection					15,18,34
NC	Signal ground					16
NC	+5V	Printer				35

etting this bit high allows it to be used as an input (SPP only)

[2]Some Data ports are bidirectional.

Parallel port register definitions

Base address: 0378h

Data Register (Base Address)					
Bit	***Pin: D-sub***	**Signal Name**	**Source**	**Inverted at connector?**	**Pin: Centronics**
0	2	Data bit 0	PC	no	2
1	3	Data bit 1	PC	no	3
2	4	Data bit 2	PC	no	4
3	5	Data bit 3	PC	no	5
4	6	Data bit 4	PC	no	6
5	7	Data bit 5	PC	no	7
6	8	Data bit 6	PC	no	8
7	9	Data bit 7	PC	no	9
Some Data ports are bidirectional. (See Control register, bit 5 below.)					
Status Register (Base Address +1)					
Bit	***Pin: D-sub***	**Signal Name**	**Source**	**Inverted at connector?**	**Pin: Centronics**
3	15	nError (nFault)	Peripheral	no	32
4	13	Select	Peripheral	no	13
5	12	PaperEnd	Peripheral	no	12
6	10	nAck	Peripheral	no	10
7	11	Busy	Peripheral	yes	11
Additional bits not available at the connector: 0: may indicate timeout (1=timeout). 1, 2: unused					
Control Register (Base Address +2)					
Bit	***Pin: D-sub***	**Signal Name**	**Source**	**Inverted at connector?**	**Pin: Centronics**
0	1	nStrobe	PC[1]	yes	1
1	14	nAutoLF	PC[1]	yes	14
2	16	nInit	PC[1]	no	31
3	17	nSelectIn	PC[1]	yes	36
[1]When high, PC can read external input (SPP only). Additional bits not available at the connector: 4: Interrupt enable. 1=IRQs pass from *nAck* to system's interrupt controller. 0=IRQs do not pass to interrupt controller. 5: Direction control for bidirectional Data ports. 0=outputs enabled. 1=outputs disabled; Data port can read external logic voltages. 6,7: unused					

Appendix B

ISA (Industry Standard Architecture) Bus

Pins layout

D	Description	Name	Pin	Pin	Name	Description	D
/	Ground	GND	B1	A1	IO CHK	I/O Channel Check	-I
O	Reset	RESET	B2	A2	SD7	System Data bit 7	I/O
/	Power +5V	+5V	B3	A3	SD6	System Data bit 6	I/O
I	Interrupt Request 9	IRQ9	B4	A4	SD5	System Data bit 5	I/O
/	Power -5V	-5V	B5	A5	SD4	System Data bit 4	I/O
I	DMA Request 2	DRQ2	B6	A6	SD3	System Data bit 3	I/O
/	Power -12V	-12V	B7	A7	SD2	System Data bit 2	I/O
/	Zero Wait State	0WS	B8	A8	SD1	System Data bit 1	I/O
/	Power +12V	+12V	B9	A9	SD0	System Data bit 0	I/O
/	Ground	GND	B10	A10	IO RDY	I/0 Channel Ready	-I
O	System Memory Write	SMEMW	B11	A11	AEN	Address Enable	O
O	System Memory Read	SMEMR	B12	A12	SA19	System Address bit 19	O
I/O	I/O Write	IOW	B13	A13	SA18	System Address bit 18	O
I/O	I/O Read	IOR	B14	A14	SA17	System Address bit 17	O
O	DMA Request Acknowledge 3	DACK3	B15	A15	SA16	System Address bit 16	O
I	DMA Request 3	DRQ3	B16	A16	SA15	System Address bit 15	O
O	DMA Request Acknowledge 1	DACK1	B17	A17	SA14	System Address bit 14	O
I	DMA Request 1	DRQ1	B18	A18	SA13	System Address bit 13	O
I/O	Refresh cycle in progress	REFRESH	B19	A19	SA12	System Address bit 12	O
O	System Clock	CLOCK	B20	A20	SA11	System Address bit 11	O
I	Interrupt Request 7	IRQ7	B21	A21	SA10	System Address bit 10	O
I	Interrupt Request 6	IRQ6	B22	A22	SA9	System Address bit 9	O
I	Interrupt Request 5	IRQ5	B23	A23	SA8	System Address bit 8	O
I	Interrupt Request 4	IRQ4	B24	A24	SA7	System Address bit 7	O
I	Interrupt Request 3	IRQ3	B25	A25	SA6	System Address bit 6	O
O	DMA Request Acknowledge 2	DACK2	B26	A26	SA5	System Address bit 5	O
O	T/C	TC	B27	A27	SA4	System Address bit 4	O
?	Buffered Address Latch Enable	BALE	B28	A28	SA3	System Address bit 3	O
/	Power +5V	+5V	B29	A29	SA2	System Address bit 2	O
O	Oscillator	OSC	B30	A30	SA1	System Address bit 1	O
/	Ground	GND	B31	A31	SA0	System Address bit 0	O

Signal Description

CLOCK (*System Drive*) output
The system clock is a synchronous microprocessor cycle clock.

RESET (*Reset Drive*) output
This signal goes high at power-up, hardware reset, or when low line-voltage occurs.

SA0 to SA19 (*System Addresses*) input/output
The system address lines run from bit 0 through 19. They are latched onto the falling edge of BALE.

SD0 to SD7 (*System Data bits*) Input/Output
System data bits 0 to 7.

BALE (*Buffered Address Latch Enable*) input
The buffered address latch enable is used in latch SA0 to SA19 on the falling edge of BALE. During DMA cycles, BALE is forced high.

IO CHK (*I/O Channel Check*) active low input
I/O channel check is active low signal which indicate that a parity error exists in the I/O board.

IO RDY (*I/O Channel Ready*) input
This signal lengthens I/O or memory cycles and should be held low with valid addresses. It can be held low for a maximum of 2.5 microseconds.

IRQ 3 to 7, 9 (*Interrupt Requests*) input
These interrupt request signals indicate I/O service request attention. They are prioritized in the following sequences: highest IRQ 9 and lowest IRQ 3, 4, 5,6,7,8.

IOR (*I/O Read*) active low input/output
Instructs an I/O device to drive its data onto the data bus.

IOW (*I/O Write*) active low output
Instructs an I/O device to read the data off the data bus.

SMEMR (*System Memory Read*) output
The system memory read signal is low while the low first megabyte memory is being read.

SMEMW (*System Memory Write*) output
The system memory write signal is low while the low first megabyte memory is being written.

DRQ 0 to 3 (*DMA Requests*) active high input
DMA Request channels 0 to 3 are for 8-bit data transfers. DRQ4 is used on the system board. Hold a DRQ line high until its DMA Request Acknowledge (DACK) goes active. Their priority is in the following sequences: highest DRQ 0,1,2, and 3.

DACK 1 to 3 (*DMA Request Acknowledges*) output
These signals are used to acknowledge the corresponding signals for DRQ 0 to 3.

AEN (*Address Enable*) output
The address enable is high when the DMA controller drives the address bus and is low when the CPU drives the address bus.

REFRESH (*Refresh cycle in progress*) active low input/output
This signal indicates a refresh cycle is in progress.

TC (*T/C*) output

OSC (*Oscillator*) output
The oscillator signal is used for the color graphic card.
High-speed clock (70 ns, 14.31818 MHz), 50%duty cycle

0WS (*Zero Wait State*) input
The zero wait state indicates to the microprocessor that the present bus cycle can be completed without inserting any additional wait cycles.