The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Bachelor of Technology - Level 05

**ECX5231 – Network Theory**
Final Examination 2008/2009

Duration: 3 hours

Date: 26.03.2009 Time: 14.00-17.00

Answer ***five*** questions selecting **at least one** question from section B. All questions carry equal marks.

## SECTION –A

**Q1.** Sparsity programming is aimed at optimizing the process of solving formulations of sparse electrical circuits. Structure of a formulation of a simple electric circuit is shown below.

$$\begin{bmatrix} x_{11} & & & & & & \\ x_{21} & x_{22} & & x_{24} & & & \\ & & x_{33} & x_{34} & & & \\ & x_{42} & x_{43} & x_{44} & & x_{46} & \\ x_{51} & x_{52} & & & x_{55} & & \\ & & x_{63} & & & & \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \end{bmatrix} = \begin{bmatrix} y_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

(a) Briefly explain what is mean by the exploitation of sparcity during circuit simulation.

(b) What are the resources that can be efficiently utilized with sparcity programming?

(c) Reorder the given system of equations to minimize the filling during the solving process.

(d) Briefly explain the role of proper storage structures in sparcity programming.

**Q2.** A simple circuit having a non linear resistor is shown in the figure Q2.

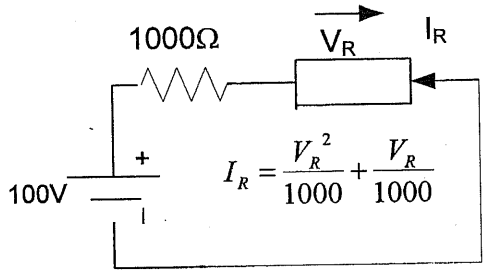


Figure Q2

(a) Represent the given circuit with the help of a companion network model of the diode

(b) Find the DC steady state voltages of the circuit by performing three iterations.(Assume initial guess as zero volts )

(c) Role of the **rich device libraries** cannot be ignored when evaluating the capabilities and performances of modern simulators.

(i) What are the essential features of a rich device library of a circuit simulator

(ii) Briefly explain how those features can be incorporated to a device library.

**Q3.** A step input having a magnitude of 5V is applied to the simple RC circuit shown in figure Q3. Assume initial voltage across the capacitor as zero.

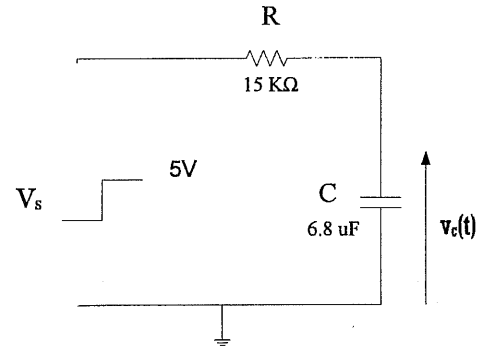


Figure Q3

(a) Represent the given circuit by replacing the capacitor with its companion network model using backward Euler formula.

(b) Obtain a formulation to the given circuit.

(c) Find the voltage across the capacitor at two time steps with $\Delta t$=10 mS.

(d) It is required to develop a transient simulation module using an available DC steady state simulation module which computes the steady voltages when a circuit description is given as its input.

(i) Represent the complete algorithm of the above mentioned implementation with additionally required functional blocks.

(ii) Briefly describe the functions of all additional blocks in the algorithm shown in the Q3.(c).i.

**Q4.** A simple passive electrical circuit is shown in figure Q4.

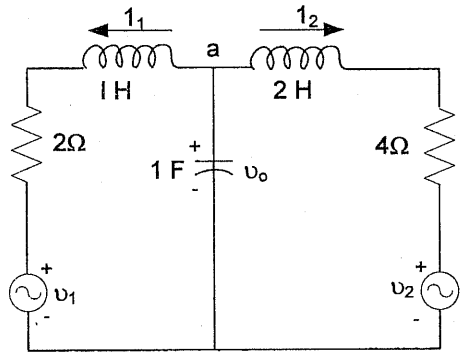


Figure Q4

(a) Obtain the matrix form of the state space equations for the circuit shown in figure Q4.

(b) Derive the transfer function $V_o(s)/V_1(s)$ using the derived state space model in Q4.(a).

(c) Briefly explain the possibility of using state space model of an electrical circuit to perform the following analysis and also state if any additional tools are required for it.

(i) Sinusoidal steady state analysis

(ii) Transient analysis

**Q5** An operational amplifier based amplifier circuit is shown in the figure Q5, given that the operational amplifier is ideal.

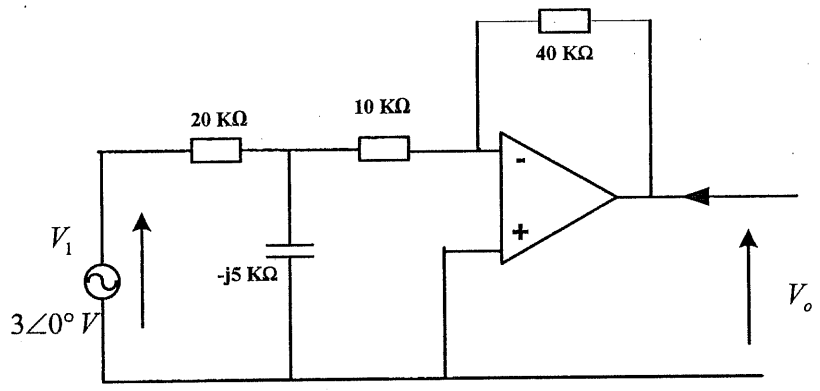


*Figure Q5*

(a) Derive the adjoint network model for the operational amplifier.

(b) Calculate the sensitivity of the output voltage $V_o$ with respect to all elements.

(c) Distinguish sensitivity analysis from tolerance analysis.

**SECTION B**

Answer the following questions with reference to the attached article (Only first four pages of the article are reproduced).

**Q6.** A circuit can be simulated on different levels and its responses viewed from different angles.

(a) Distinguish device simulation from circuit simulation. Dose this article mainly concentrate on device simulation or circuit simulation? Justify your answer.

(b) Distinguish modulo approach of circuit analysis from the holistic approach. What is the approach used to perform small signal analysis of semiconductor devices in the given article?

**Q7.** The article describes several methods of small signal analysis of semiconductor devices.

(a) Sketch the functional block diagram of the algorithm for the small signal semiconductor device analysis process called **Fourier decomposition of transient excitation (FD) method** described in the article.

(b) Briefly explain the strengths and limits of the FD method

**Q8.** Modern circuit simulators consist of many computer tools and techniques. They are more capable and efficient than the early simulators. This development is due to the development of many circuit simulation techniques as well as the developments in some other fields of studies. One example is given in the article.

(a) List four tools and techniques in the field of electrical engineering or any other field of study that led to the development of simulation packages.

(b) Briefly explain two of them.

IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN, VOL. CAD-4, NO. 4, OCTOBER 1985

# Techniques for Small-Signal Analysis of Semiconductor Devices

STEVEN E. LAUX

*Abstract*—**Techniques for ascertaining the small-signal behavior of semiconductor devices in the context of numerical device simulation are discussed. Three standard approaches to this problem will be compared: (i) transient excitation followed by Fourier decomposition, (ii) incremental charge partitioning, and (iii) sinusoidal steady-state analysis. Sinusoidal steady-state analysis is shown to be the superior approach by providing accurate, rigorously correct results with reasonable computational cost and programming commitment.**

## Introduction

COMPUTER codes providing steady-state (dc) and transient solutions to the semiconductor transport equations in multiple-space dimensions are fast becoming a standard tool for device design. The literature on numerical device simulation addressing steady-state and transient device solutions is voluminous and ever growing (e.g., [1], [2], and references therein). A third device operating mode, namely small-signal ac operation, has received somewhat less attention to date in the context of numerical device simulation. While excellent work has appeared concerning ac simulation of one-dimensional devices [3]–[7], progress in ac simulation of devices in multiple space dimensions has been somewhat slow by comparison. This is due partly to the need to have an existing dc device solution upon which to build the small-signal ac analysis and partly to the nature of the ac computation.

Fourier decomposition techniques were first invoked to numerically characterize the ac behavior of a two-dimensional device [8]. However, many time steps are necessary to obtain sufficient time-domain accuracy to generate sufficient frequency-domain accuracy. Because of the multi-dimensional nature of the problem and the computer technology at the time, the computational intensity of this transient simulation encouraged other approaches to the ac problem. A second approach based upon incremental charge partitioning heuristics evolved. Such heuristics are often posed in the context of a specific analytic device model [9]–[12] but such partitioning of incremental charge can readily be adapted to the interpretation of numerical device simulation results. Incremental charge partitioning heuristics have also been attempted using a device independent approach [13], [14]. In every case, the results can be quite accurate and computationally inexpensive; however, a rigorously correct charge partitioning scheme suitable for implementation into a universal device simulation code remains an open question. Recently, sinusoidal steady-state analysis has been demonstrated in a two-dimensional bipolar simulation code [15], [16] and then in the universal two- and three-dimensional device simulation code FIELDAY [17]. Using sinusoidal steady-state analysis, the small-signal ac behavior of a device can be determined with far less cost compared to transient excitation followed by Fourier decomposition. Results from sinusoidal steady-state analysis give an accurate and rigorously correct relationship between sinusoidal terminal voltages and currents; furthermore, the analysis is naturally incorporated into a universal device simulation code.

After defining the ac simulation problem, the three aforementioned approaches to ascertaining small-signal ac device behavior in the context of numerical device simulation will be discussed in turn. Both transient excitation followed by Fourier decomposition (FD) and incremental charge partitioning heuristics (CP) will be discussed in sufficient detail to support a comparison of the three methods and to substantiate the superiority of sinusoidal steady-state analysis ($S^3A$). As a specific example, the ac behavior of a 1-$\mu$m n-MOSFET obtained using $S^3A$ will be described.

## Problem Definition

Small-signal ac device characterization implies ascertaining the relationship between "small" sinusoidal terminal currents and voltages superimposed upon an established steady-state (dc) device bias. Here "small" means in the limit of infinitesimal amplitude so that no harmonic generation occurs within the device. This relationship must be characterized as a function of frequency and as a function of dc operating point. Direct inclusion of harmonic generation using $S^3A$ has been reported in a one-dimensional simulation [18]; however, large-signal ac behavior including harmonic generation is beyond the scope of this work. The effects of harmonic generation within the device can often be estimated by a parametric study of small-signal ac behavior versus dc bias, however.

Small-signal ac device characterization permits many useful device attributes to be calculated such as voltage gain $A_V$, current gain $A_I$, unity current gain frequency $f_T$ and the gain–bandwidth product as well as allowing estimates of stability and noise behavior. Information from ac analysis can greatly assist in distilling off detailed behavior

Manuscript received January 2, 1985; revised May 9, 1985.

The author is with IBM Thomas J. Watson Research Center, Yorktown Heights, NY 10598.

0278-0070/85/1000-0472$01.00 © 1985 IEEE

obtained from full device simulation to obtain concise circuit-level descriptions of device behavior. Furthermore, ac characterization of devices in the laboratory is commonplace; direct simulation of ac behavior is mandated for this reason as well. Given the wealth of information obtainable from ac analysis, the topic is of interest to both analog and digital device designers.

Having embraced the small-signal assumption, the ac behavior of a (now linear) $N$-terminal device is concisely expressed as a $N \times N$ matrix of complex numbers relating the phasor terminal voltages $\tilde{V}_i$, $i = 1, \cdots, N$ and phasor terminal currents $\tilde{I}_i$, $i = 1, \cdots, N$ [19]. Note that the tilde denotes a complex quantity. While many choices are possible, the admittance formulation is convenient since device simulation programs most commonly use a voltage drive and calculate a current response. The $N \times N$ admittance matrix $\tilde{Y}$ is defined by

$$\tilde{I} = \tilde{Y}\tilde{V} \tag{1}$$

where $\tilde{I} = [\tilde{I}_1, \cdots, \tilde{I}_N]^T$ and $\tilde{V} = [\tilde{V}_1, \cdots, \tilde{V}_N]^T$. The real and imaginary parts of the admittance matrix determine the conductance matrix $G$ and the capacitance matrix $C$ via $\tilde{Y} = G + j\omega C$, where $j = \sqrt{-1}$ and $\omega$ is the radian frequency. As there is no absolute voltage reference for the $N$-terminal device, each row of $\tilde{Y}$, $G$, and $C$ sums to zero. Similarly, as ac current continuity holds, each column of $\tilde{Y}$, $G$, and $C$ also sums to zero [20]. In view of these two constraints on the matrix entries, there are only $(N-1)^2$ independent entries in each of $\tilde{Y}$, $G$, and $C$. Individual matrix elements are readily determined by exciting the device with a single voltage perturbation $\tilde{V}_j$, namely

$$\tilde{Y}_{ij} = \left.\frac{\tilde{I}_i}{\tilde{V}_j}\right|_{V_k=0, k\neq j}. \tag{2}$$

In summary, the small-signal device ac admittance matrix (or an equivalent network matrix) is sought from each of the three analysis methods.

## Fourier Decomposition of Transient Excitations (FD)

Transient excitation of a device followed by Fourier decomposition is a straightforward technique for finding the ac behavior of a simulated device [8]. An obvious prerequisite is the availability of a transient device simulation code. Let a "small" perturbation in voltage be applied to contact $j$ at $t = 0$. Let the total current (voltage) at contact $m$ be denoted by $i_m(t)\,(v_m(t))$ and the initial dc current (voltage) be given by $I_m(0)\,(V_m(0))$. The small-signal admittance matrix component $\tilde{Y}_{ij}$ as a function of frequency is given by

$$\tilde{Y}_{ij} = \frac{\mathcal{F}\{i_i(t) - I_i(0)\}}{\mathcal{F}\{v_j(t) - V_j(0)\}}. \tag{3}$$

For simplicity, let the voltage perturbation be a step of amplitude $\Delta V_j$; hence, $v_j(t) = V_j(0) + \Delta V_j u(t)$. Substituting the Fourier decomposition of the step function into (3) and separating into frequency dependent and independent parts

$$\tilde{Y}_{ij} = \frac{I_i(\infty) - I_i(0)}{\Delta V_j} + \frac{j\omega}{\Delta V_i}\mathcal{F}\{i_i(t) - I_i(\infty)\} \tag{4}$$

where the final dc value of the current at contact $i$ is given by $I_i(\infty)$. Upon separating (4) into real and imaginary parts, the conductance and capacitance matrix entries become

$$G_{ij} = \left\{\frac{I_i(\infty) - I_i(0)}{\Delta V_j} + \frac{\omega}{\Delta V_i}\int_0^\infty [i_i(t) - I_i(\infty)]\sin \omega t\, dt\right\} \tag{5a}$$

$$C_{ij} = \left\{\frac{1}{\Delta V_j}\int_0^\infty [i_i(t) - I_i(\infty)]\cos \omega t\, dt\right\}. \tag{5b}$$

Equation (5) simplifies for very low frequencies to become

$$G_{ij}(\omega \to 0) = \frac{I_i(\infty) - I_i(0)}{\Delta V_j} \tag{6a}$$

$$C_{ij}(\omega \to 0) = \frac{1}{\Delta V_j}\int_0^\infty [i_i(t) - I_i(\infty)]\, dt. \tag{6b}$$

In the limit of zero perturbation amplitude, method FD as described is trivially shown to rigorously determine the small-signal device admittance matrix defined in the previous section. Variations on the above formulas are possible, however. Excitations other than a step function may be used. Fast Fourier transform methods may be used in evaluating the indicated integrals. The following comments on FD remain invariant with these alterations.

In order to generate sufficient output signal at the highest frequency of interest $f_h$, the time step $\Delta t$ used for transient simulation must obey $\Delta t << (2\pi f_h)^{-1}$. This sets an upper bound on the selection of the first few time steps. There is also a lower bound constraining the value of the first few time steps in the transient simulation. This can be seen as follows. Due to the feedback capacitance present in the intrinsic device, a transient spike appears at time $t = 0^+$ in the terminal currents. This current spike is proportional to the time derivative of the applied voltage perturbation and is pure displacement current. For a step function in discrete time (thus actually a ramp function), this spike amplitude is proportional to $(\Delta t)^{-1}$. The time step $\Delta t$ must be chosen to enable total current continuity to be maintained throughout the simulated transient, i.e., during *and* after the current spike. The spike amplitude must not be so large as to force a loss of current continuity due to the finite computer word length after the spike disappears. For example, a typical dc solution using FIELDAY maintains current continuity to ten decimal digits. For a transient simulation, the initial $\Delta t$ is chosen to cause the current spike to exceed the baseline transient current by 4 orders of magnitude, leaving 6 decimal digits of current continuity immediately after the disappearance of the spike. After a few time steps, a full ten digits of

current continuity are once again obtained. Note proper resolution of this current spike is imperative if the feedthrough component of the total capacitance is to be properly resolved. In some cases, the feedthrough component can be 50 percent of the total internodal capacitance as will be seen in the n-MOSFET example in the final section.

Avoiding this current spike may seem desirable. This can be done by driving the transient system with current instead of voltage [21]. Using a ramp or other voltage perturbation does not avoid generation of the current spike. Slowing down the rise time of the voltage perturbation does decrease the spike amplitude, but this rise time must not slow to the point where the feedthrough capacitance is ill-resolved in the Fourier decomposition. As simulating the current spike has never posed a problem, step-function voltage perturbations are used exclusively for FD. The specific value of initial $\Delta t$ required is problem dependent but typically ranges from 1 to 100 fs.

Selection of the voltage step amplitude $\Delta V_j$ is more straightforward. $\Delta V_j$ must be sufficiently large to dominate numerical noise and convergence criteria uncertainty present in the calculation. In addition, $\Delta V_j$ must be sufficiently small so as to avoid harmonic generation in the device response. A specific value of $\Delta V_j$ is difficult to generalize but values typically range from 10 to 100 mV.

The net of this discussion is that FD is a viable means to ascertaining ac device behavior. The major disadvantage with the method is summarized in Fig. 1. Error in low frequency capacitance (6b) versus total number of time steps used is shown for a one-dimensional MOS capacitor biased at flatband. The oxide thickness is 25 nm and the silicon is uniformly doped $N_D = 1 \times 10^{15}$ cm$^{-3}$. The silicon is 3.0 $\mu$m in length. An analytic $C_{FB}$ for a capacitor of infinite length is known [22] for comparison. For each transient simulation underlying a data point in Fig. 1, the first two time steps are the same ($2 \times 5$ fs) allowing proper resolution of the transient displacement current spike. The remaining timesteps increase exponentially with time which maintains the local temporal truncation error approximately constant throughout the transient. Normalized temporal truncation errors range from 0.05 to 0.0007 for the coarsest to finest time discretizations, respectively. A standard first-order accurate backward Euler time discretization is used. Fig. 1 indicates greater than 300 timesteps are required to determine $C_{FB}$ to within a 1-percent error. Note for this first order accurate time discretization, the error in $C_{FB}$ is approximately inversely proportional to the number of time steps used. Fewer time steps will certainly be required to achieve this same accuracy with a higher order time stepping scheme. To obtain ac information as a function of dc bias, transient simulation(s) is required at each dc bias of interest. A *single* FD of a voltage perturbation will provide the frequency dependence of *one* column in $\tilde{Y}$. For an $N$-terminal device, $N-1$ transient excitations are required to determine $\tilde{Y}$ at a given dc bias point. The remaining column of $\tilde{Y}$ is found from the zero summing property of the rows of $\tilde{Y}$. The

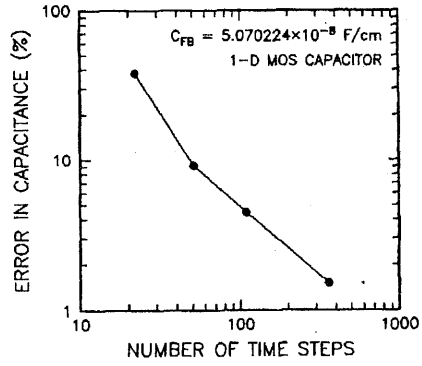


Fig. 1. Error in flatband capacitance obtained using FD versus number of time steps for a 1-D MOS capacitor.

computational intensity of this entire process for a two- or three-dimensional device geometry is thus extrapolated to be quite severe.

It is this computational intensity which represents the major disadvantage to using FD in ascertaining ac device behavior. Time step selection primarily determines the accuracy of the final admittance matrix. Unfortunately, this implies accuracy of the admittance matrix is directly proportional to the time required to compute the device transient response.

## Incremental Charge Partitioning (CP)

The incremental charge partitioning approach to ascertaining ac device behavior poses little computational burden and requires only a dc simulation code as a prerequisite. The approach can yield reasonable results; however, only in rare cases is the capacitance matrix rigorously correct. In every case, incremental charge obtained from steady-state device simulation is partitioned and therefore only quasi-static (i.e., the low-frequency limit) admittance is determined.

The basis for CP can be inferred from (6) obtained using FD. The application of a voltage perturbation $\Delta V_j$ to contact $j$ is again involved; however, for CP *no* device information is available from the ensuing transient response of the device. Only steady-state information is available which corresponds in FD nomenclature to the initial and final states of the device. Following (6a), the quasi-static conductance matrix does not depend on the intervening transient response of the device. As a result, the quasi-static conductance matrix can be rigorously obtained by forming ratios of the incremental change in terminal current to the applied voltage perturbation amplitude as in (6a). The quasi-static conductance matrix obtained is identically equal to the quasi-static conductance matrix from method FD and is, therefore, rigorously correct.

Determination of quasi-static capacitance does depends on the transient response of the device, however, as seen in (6b). CP finds the capacitance matrix component using the formula $C_{ij} = \Delta Q_i / \Delta V_j$, where $\Delta Q_i$ is some incremental charge associated with contact $i$. By equating this formula with (6b), $\Delta Q_i$ becomes

$$\Delta Q_i = \int_0^\infty [i_i(t) - I_i(\infty)]\, dt. \tag{7}$$

In general, this integral is impossible to evaluate from only initial and final value data. An important exception is the case when $i_i(t)$ is solely displacement current. This occurs, for example, when contact $i$ is the gate of a MOSFET. In this case, $I_i(\infty) \equiv 0$ and

$$i_i(t) = \oint_{\text{gate}} \epsilon_{\text{ox}} \frac{\partial \vec{E}}{\partial t} \cdot \hat{n}\, dl \tag{8}$$

where $\epsilon_{\text{ox}}$ is the gate oxide permittivity, $\vec{E}$ is the electric field and $\hat{n}$ is the unit vector normal to the gate contact. Inserting (8) into (7) allows the time integral of (7) to "undo" the time derivative of (8). The incremental charge $\Delta Q_i$ in this case just becomes the incremental charge induced on the gate contact by the dc voltage perturbation. The integration of incremental charge induced on the gate is readily accomplished. Thus $C_{GX}$, where $G$ denotes the gate and $X$ denotes any other MOSFET contact, can be simply and rigorously computed with CP.

If the current at contact $i$ is not solely displacement current, physical insight into device operation may still allow the integral of (7) to be approximated. In the simple case of a one-dimensional p-n-junction under reverse bias, a dc bias perturbation causes the charge at the depletion region edges to change incrementally. This incremental charge is supplied to the device through the contacts, each contact responding to the charge requirements of the nearest depletion edge. Such insight can be used as follows. If contact $i$ supplies incremental charge to a certain portion of the interior of the device, this incremental charge can be summed and associated with contact $i$. Such a summation will give an approximation to $\Delta Q_i$ and thus $C_{ij}$. The result can be a good approximation to $\Delta Q_i$ if the incremental charge summed is known to associate with contact $i$ and no other contact. For the one-dimensional p-n junction, this assumption is excellent in reverse bias. In forward bias, however, the depletion width shrinks and the incremental charge at each depletion edge overlaps. This makes unique association of incremental charge with a contact difficult [23].

For arbitrary $N$-terminal devices, such physical insight is rarely available. For more conventional embodiments of a $N$-terminal device such as the four terminal MOSFET, however, some guiding insight is available. For example, $C_{GX}$ can be rigorously determined as seen previously. Current entering the backside contact provides carriers which incrementally modulate the depletion region edge beneath the source, gate and channel. Charge entering the source and drain primarily feed the channel, although the relative contributions from source and drain are not easily estimated. Such a device specific approach [9]–[12] can yield acceptable results, is readily adapted to analyzing results obtained from numerical device simulation and has negligible computational burden. However, an extension of the CP method as described for inclusion into a universal device simulation code is desirable.

Extending the basic CP idea expressed above to the general $N$-terminal device has been attempted [14]. The findings of this study will be summarized here. The precept is to use the internal device solution obtained from simulation to determine not only the amount of incremental charge within the device but also how this charge is to be associated with device contacts. Consider the incremental charge within a device partitioned by arithmetic sign, that is, divide the device into two areas where charge either increased or decreased in response to a voltage perturbation. This partition is a heuristic proposed in analogy to the arithmetic sign of the incremental charge on the two plates of a parallel-plate capacitor. These two partitions of incremental charge need now to be associated with two device contacts. This immediately leads to viewing the $N$-terminal device as a two-terminal equivalent with each of the $N$-terminals assigned to one or the other terminal in the equivalent device. A device independent CP algorithm might proceed as follows: (i) consider the $N$-terminal as an equivalent two-terminal device; (ii) apply the same voltage perturbation to each of the $N$-terminals assigned to the first contact of the equivalent device; (iii) partition the internal incremental charge (including charge induced on contacts) by arithmetic sign and sum up the charge in the two regions; (iv) determine an effective capacitance given by the ratio of incremental charge to voltage increment; (v) equate this effective capacitance to an appropriate sum of $C_{ij}$'s. This sum of $C_{ij}$'s is found from the $N$ matrix equations $(\Delta Q) = C(\Delta V)$ by summing together individual entries in the $(\Delta Q)$ column vector according to the $N$-terminal correspondence with the two-terminal equivalent expressed by the $(\Delta V)$ column vector.

This heuristic for device independent CP can be readily implemented in the context of numerical device simulation of an arbitrary $N$-terminal device. The algorithm has two flaws. First, device *specific* CP is unable to always approximate the integral of (7); device *independent* CP is not expected to avoid this limitation. The charge partition based on arithmetic sign has been not rigorously derived and hence will also be in error with respect to (7). The extent of this error is, unfortunately, very device specific. Secondly, the number of independent combinations of an $N$-terminal device viewed as a two-terminal equivalent is $0.5N(N-1)$. If $N > 2$, this is less than the number of independent entries in the capacitance matrix, namely, $(N-1)^2$. If an independent source of information relating $C_{ij}$ and $C_{ji}$ for the $N > 2$ terminal device were found, this shortfall would exactly be rectified. Unfortunately, an independent relationship characterizing the extent of nonreciprocity in the capacitance matrix is not known in general. If no dc current flows in the device, $C_{ij} = C_{ji}$ [24] but this situation is rarely of interest.

In summary, the device specific CP method is viable for determining ac device behavior in the context of numerical device simulation. The computational burden is trivial, only a dc simulation code is required and the necessarily quasi-static results can be quite accurate if changes within the device can be partitioned based on sound physical