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The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination –2008
ECX 6330 – Electronic Systems **(Closed Book)**

Time: 0930-1230hrs. Date: 20.04.2009

Answer any five questions.

1. A differential amplifier circuit is shown in Figure-Q1. The two transistors are matched and the base currents can be neglected.

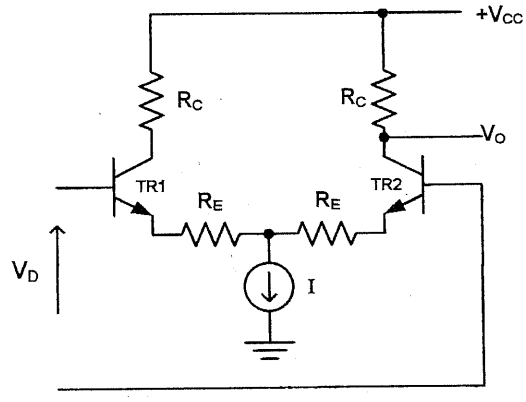


Figure - Q1

(a) Draw the ac equivalent circuit for TR2 (half circuit) using the small signal transconductance model of a transistor. Hence find an expression for the voltage gain $\frac{v_o}{v_D}$ in terms of g_m, R_C and R_E, where g_m is the transconductance of a transistor.

(b) You are required to design an amplifier using this circuit to have a gain $\frac{v_o}{v_D}$ of 18. When considering linearity issues, maximum signal voltage between base and emitter is limited to 6mV. The quiescent collector current of each transistor is 0.4mA. If the maximum amplitude of the output signal is 4V, find values for R_C, R_E and I. You may assume that the room temperature is 25^0C.

(c) Draw the transconductance model for your amplifier and calculate the parameters of the model from the values obtained in (b). If the amplifier is connected to a 100K load, calculate the resulting voltage gain.

2. (a) State an advantage of a class AB amplifier over a class B amplifier.
(b) Consider the power amplifier circuit shown in Figure-Q2. Biasing arrangement of the circuit is not shown for simplicity.

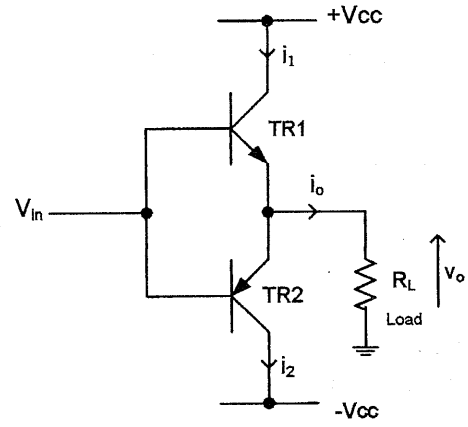


Figure - Q2

(i) Sketch i_1, i_2, i_o and v_{in} on a common time scale.

(ii) If the output signal of the amplifier is given by $v_o = A\,Sin\,\omega t$, derive expressions for the output power and for the power dissipated at the transistors.

(iii) Find the maximum power delivered to the load and the maximum power dissipation at the transistors.

(iv) Find the maximum and minimum conversion efficiencies of the circuit and the corresponding amplitudes of the output signal.

(v) Analyze this circuit for thermal safety and give recommendations for safe operation using the following data. Assume usual notation.

$V_{CC} = 24V$ $R_L = 3\Omega$ $T_a(\max) = 40\ ^0C$ $T_j(\max) = 200\ ^0C$

$\theta_{jC} = 3\frac{^0C}{W}$ $\theta_{ca} = 10\frac{^0C}{W}$

3. A high gain multistage amplifier consists with four cascaded stages as shown in Figure – Q3, in which the first stage is a differential amplifier. The input and output resistance of each stage with the equivalent capacitance is shown in the figure, while A_1, A_2, A_3 and A_4 are the gains of each stage respectively.

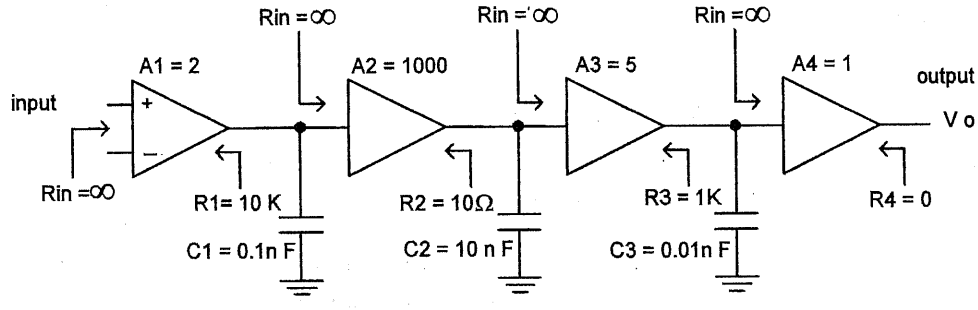


Figure - Q3

(a) Derive the overall open loop gain A(s) and then sketch the magnitude and phase Bode plots of the gain transfer function in the frequency range 10^3 to 10^9 rad/s. Indicate the slopes and label the gain levels. Use the log graph provided in the last page of the question paper. You may use the scales 1"= 40dB and 1"= 90^0.

(b) If this amplifier is provided with negative feedback having a feedback factor of 0.001, determine the gain and phase margin using (a).

(c) Find a compensation network based on pole-zero method to have a phase margin of 45^0 with a feedback factor 0.1.

4. An operational amplifier circuit is shown in Figure-Q4. You may assume that the open loop gain and the bandwidth of the amplifier as infinite.

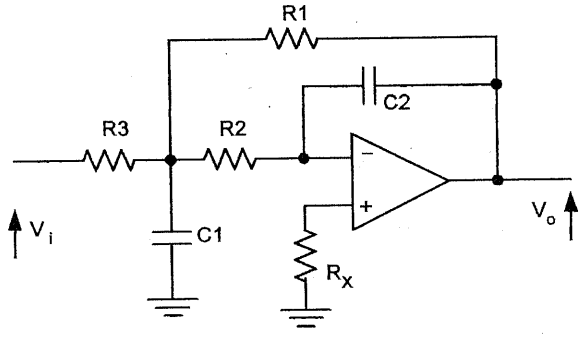


Figure - Q4

(a) Derive the voltage transfer function H(s) for this circuit.

(b) Find R_X in order to have minimum output voltage errors due to the input bias currents.

(c) Compare H(s) with the function $\frac{H_o\omega_o^2}{s^2+\alpha\omega_o s+\omega_o^2}$ and find out C_1, C_2 and H_o in terms of R, α and ω_o where R is given by $R = R_1 = R_2 = R_3$.

(d) It is required to design a second order Chebyshev low pass filter with 0.5dB of pass band ripple using the above circuit. The cut off frequency of the filter is 10 kHz. Derive the component values using the results obtained in (c) while showing frequency and magnitude scaling clearly.
The frequency normalized Chebyshev polynomial for 0.5dB pass band ripple is given by,
$s^2 + 1.4256s + 1.5162$.

5. A common base amplifier is shown in Figure-Q5(a).

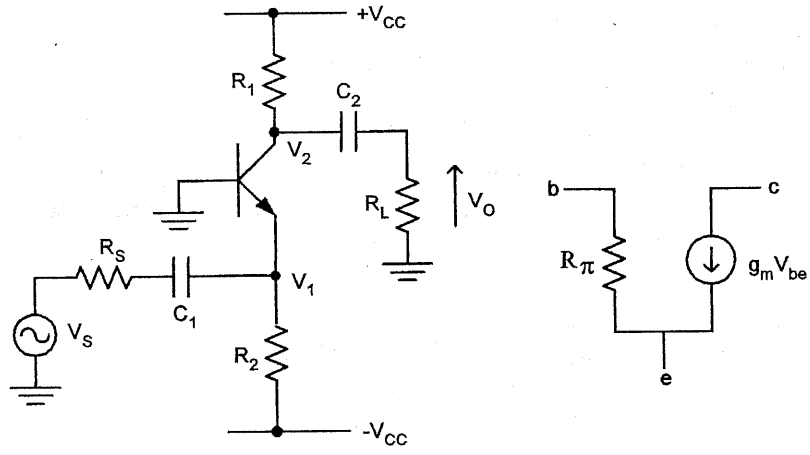


Figure - Q5

(a) Draw the ac equivalent circuit of this amplifier for <u>low frequencies</u> using the hybrid-π model shown in Figure-Q5(b).

(b) Derive the voltage gains $\frac{v_o}{v_2}$, $\frac{v_2}{v_1}$ and $\frac{v_1}{v_S}$ using this equivalent circuit at low frequencies. Hence show the gain transfer function $\frac{v_o}{v_S}$ is given by

$$\frac{v_o}{v_S} = \frac{g_m R_1 R_E R_L}{(R_1+R_L)(R_E+R_S)} \times \frac{\frac{s}{\omega_1}}{(1+\frac{s}{\omega_1})} \times \frac{\frac{s}{\omega_2}}{(1+\frac{s}{\omega_2})}, \quad \text{where } R_E = R_2 // R_\pi // \frac{1}{g_m}.$$

Derive the two corner frequencies of the gain magnitude function.

(c) Calculate the 3-dB low frequency bandwidth and the mid band gain for the following values.

$R_1 = 5.6K$ $R_2 = 2.2K$ $R_S = 75\Omega$ $R_L = 1K$ $R_\pi = 1K$

$g_m = 40$ mA/V $C_1 = 10\ \mu F$ $C_2 = 1\mu F$

6. A successive approximation type analog to digital converter is shown in Figure-Q6. The digital output is unsigned and taken from the output of the SAR. You may assume usual terminology.

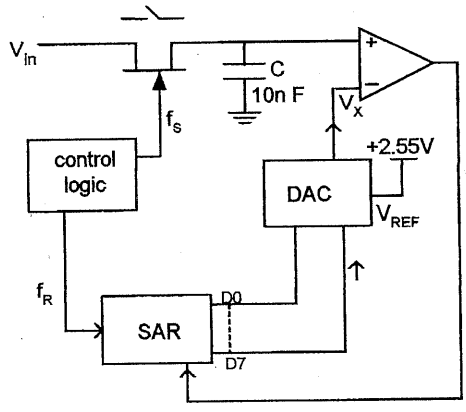


Figure-Q6

(i) Determine the resolution of this ADC. What is the digital output for an input voltage of 1.533V? Show the conversion sequence for this input by tabulating the digital output and V_X against the clock f_R.

(ii) The sampling gate takes 50ns to close and the propagation delay of SAR, DAC and the comparator are 100ns, 125ns and 50ns respectively. Calculate the minimum conversion time and the maximum frequency of the clocks f_S and f_R. You may neglect the delay in the control logic.

(iii) If the input bias current of the comparator is 4μA, calculate the voltage droop at the non-inverting input during a conversion. If the DAC has an error of 0.1% full scale and the minimum input differential voltage of the comparator required for transition is 1mV, estimate the accuracy of the ADC.

7. Design a synchronous finite state machine (FSM) to detect the bit sequence 10101 in a serial binary data stream. The circuit must be capable of detecting the sequence even for the over lapping instances.

(a) Draw the state diagram of your design.

(b) Draw the state table free of any equivalent states.

(c) Give the logic design and implementation using D flip-flops with minimum number of gates. Use any unused states for minimization and then verify the proper operation of the FSM.

(d) How many outputs to be ignored at the start to have guaranteed results?

8. The circuit shown in Figure-Q8 can be used to generate a binary sequence.

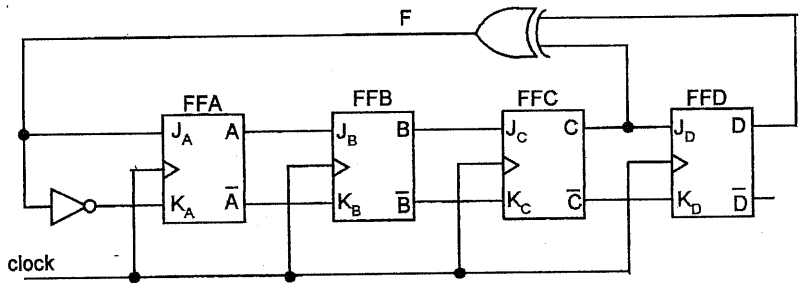


Figure - Q8

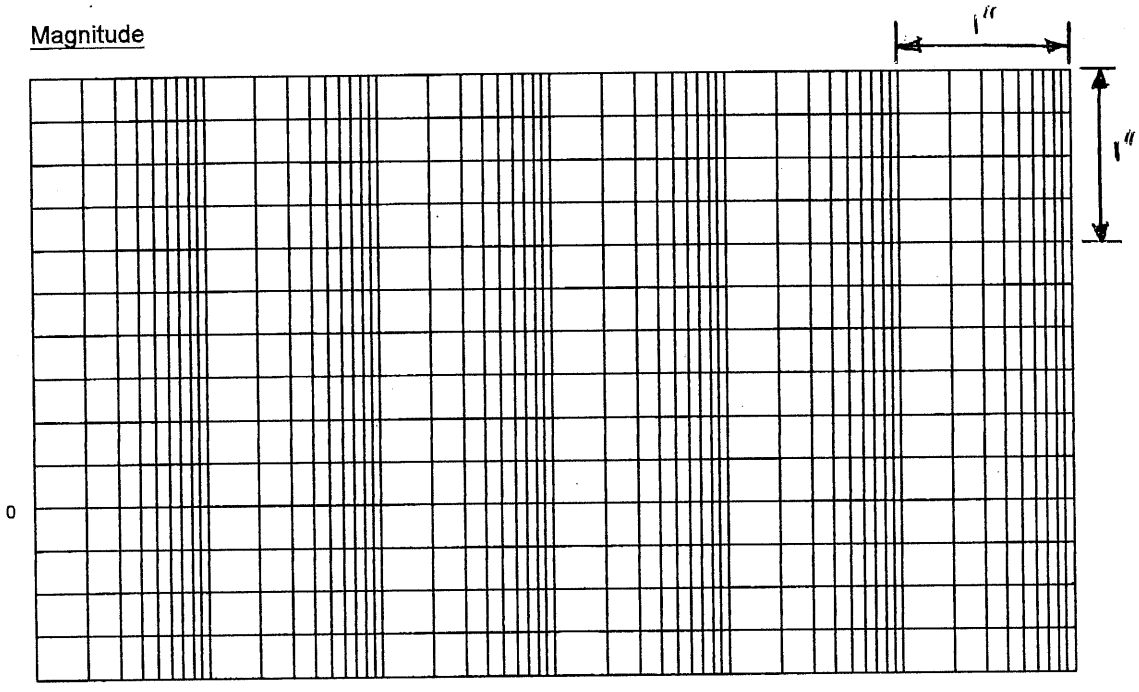
(a) Tabulate clock, A, B, C, D and F to find out the length (number of states entered before repetition) of the sequence. Assume that the initial state is DCBA = 0001.

(b) Design a logic circuit with basic gates which can be used to modify the above circuit to enter 0001 state just after power up. Your design must have a minimum number of gates and the binary sequence in (a) should not be changed. Show the design steps clearly.

(c) Calculate the maximum clock frequency for your design if the propagation delay of a flip-flops is $t_p = 8ns$ while the setup and hold times are $t_s = 5ns$ and $t_h = 2ns$. Assume that the inverters and the gates have a propagation delay in the range $15ns < t_g < 25ns$ and the clock is symmetrical with period T. Verify whether the hold time requirement is fulfilled.

Use this page for Question -3.

Magnitude



Phase