The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Bachelor of Technology - Level 05

ECX5231 – Network Theory
Final Examination 2010/2011

Duration: 3 hours

Date: 02.04.2010 Time: 14.00-17.00

This paper consists of eight questions over two sections. All questions carry equal marks.
Answer five questions selecting at least two questions from section B

Section A

Q1. The circuit shown in the figure Q1 represents small signal equivalent circuit of an FET amplifier.

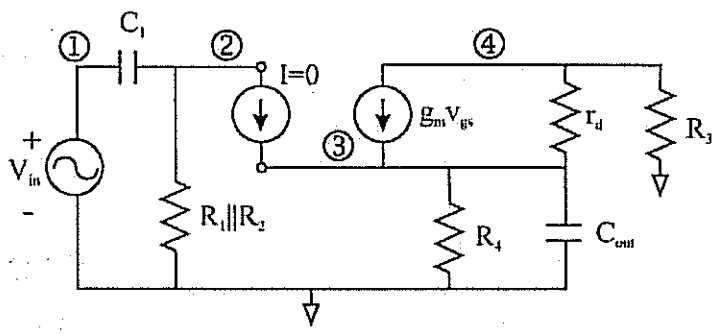

Figure Q1

(a) Write stamps of the capacitor C_1, resistor R_4, and volatge control voltage source which represents operational charaterisctics of the JFET.
(b) Formulate the circuit with help of stamps of the circuits
(c) Briefly explain the importance of using proper data structures to represent circuit equations for efficient circuit simulation

Q2. A simple circuit having a non linear resistor is shown in the figure Q2.

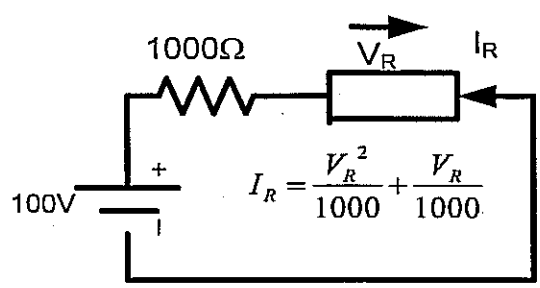

Figure Q2

(a) Represent the given circuit with help of companion network model of the non linear circuit element

(b) Formulate the circuit for DC steady state simulation

(c) Find the DC steady state voltage across the non linear element of the circuit by performing two iterations.(Take initial guess for the voltage across non linear element as ten volts)

Q3. Use companion network approach to find the step response of the circuit shown in the figure Q3.

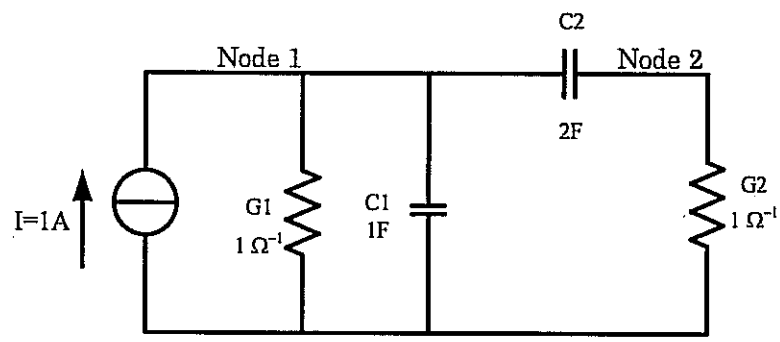

Figure Q3

(a) Determine the companion network models of capcitors using backward Euler formular.

(b) Obtain a formulation for the circuit by replacing capcitors by their campanion network models derived in Q3.(a).

(c) Find numerical solution to the voltages at node I and node 2 at 200 ms and 400 ms after aan unit step current input at the input by assuming initial capacitor voltages as zero and taking 200ms time steps.

Q4 State space formulation is extensively used to represent dynamical systems analysis.

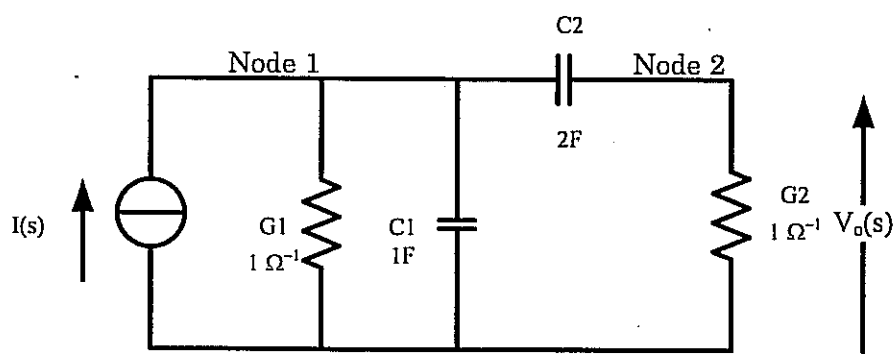

Figure Q4

(a) Formulate the node I and 2 voltages with help of nodal equations

(b) Obtain state space representation of the given circuit by selecting node volatge V_1 and V_2 as state variables .

(c) Find the transfer function between the current source and output voltage

Q5. An operational amplifier based amplifying circuit is depicted in the figure Q5, given that the operational amplifier is ideal.

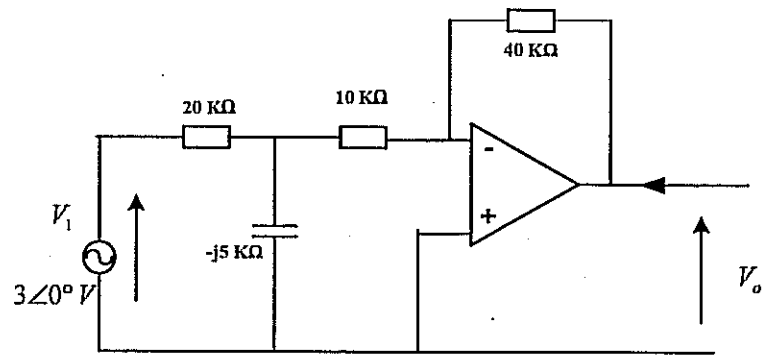

Figure Q5

(a) Draw the adjoint network model of the circuit given in Figure Q5.
(b) Obtain solutions for the circuit shown in figure Q5 and adjoint network model of the circuit
(c) Hence calculate the sensitivity of the output voltage Vo with respect to all elements.

Section B

First four pages of a research paper which summarize the current statues of power electronic devices modeling is attached at the end of this question paper. Refer the article before answering following questions.

Q6. There are some differences and similarities of the process of simulating standard low power electronic circuit and power electronic device/circuit. Answer following questions with reference to the power electronic device/circuit simulation.

(a) Distinguish power electronic circuit simulation from standard low power circuit simulation.
(b) Briefly explain the role of power electronic device/circuit simulation in the power industry.
(c) Briefly describe the necessity of more advanced device models for present power electronic circuit simulation.

Q7. Modeling is the first step of simulation which significantly determines the overall accuracy as well as the speed of simulation. Answer following question with reference to the modeling phenomena's occurred within devices which are explained in the article.

(a) Distinguish charge storage effect from the MOS capacitive effect of the semiconductor devices
(b) Briefly describe the most specific effect that is to be modeled in power electronic device simulation which is usually ignored in the standard low power device/circuit simulation
(c) List the phenomena/(s) that have to be modeled in steady state simulation of a power electronics circuits

Q8.Efficiency of simulation is not just depend on modeled effects and accuracy of modeling. Modeling approach considerably determines the efficiency.

(a) Compare *sub circuit modeling* with *mathematical functional modeling* of semiconductor devices

(b) Briefly describe why lookup table method is unsuitable for dynamic effect simulation

(c) Briefly explain advantage of using empirical equations to simulate device responses.

Status and Trends of Power Semiconductor Device Models for Circuit Simulation

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Abstract—**The current status of research in the field of power semiconductor device models is reviewed. For this purpose, the basic modeling problems and research issues, which have to be overcome in this field, are discussed. Recently, some new and quite promising modeling concepts have been proposed, which are compared with more traditional ways of achieving an efficient tradeoff between the necessary accuracy, required simulation speed, and feasibility of parameter determination. From this comparison, a prediction of the future evolution of circuit simulation models for power semiconductor devices naturally emerges. Many of the different concepts are expected to survive only in an application niche, where their specific points of strength are important. However, three modeling concepts have already been proven to be successfully applicable to the complete spectrum of power semiconductor devices and have their strength for different grades of complexity of the power circuit. A revolutionary development from anticipated or long-due breakthroughs is on the other hand not expected in the foreseeable future.**

Index Terms—**CAD, circuit simulation, modeling, parameter extraction, power semiconductor devices.**

I. Introduction

In RECENT years, research on power semiconductor device models for circuit simulation has intensified. Several research groups throughout the world have tried to advance the state of the art with respect to the status summarized in previous review articles [1], [2]. A number of new concepts for trimming the basic physical equations to the requirements of a power semiconductor device model for circuit simulation have been proposed [42], [43], [53], [69], [75], [101], [117], [119], [122], [129], [134], [140]. The special challenge in developing such models for circuit simulation results from the need to simultaneously fulfill contradicting requirements like high quantitative accuracy, low demand of computation power, and physical and easy accessible model parameters. At least a favorable tradeoff between these contradicting requirements is necessary.

Responsible for the above development are the general economical boundary conditions, which also demand an improved efficiency and reliability in the design and realization of power electronic circuits. Such an improvement can only be achieved through an upgrading of the computer-aided design (CAD) methodology and their application from the beginning of the development phase of a power electronic circuit. A key element for achieving such an upgrade in CAD methodology is the availability of high-quality power device models for circuit simulation.

Traditionally, the design tools for power circuits have employed very simple power semiconductor models, which only featured a digital switching (abrupt or linear) behavior as well as a fixed resistance in the conducting state. This standard is far below the state of the art in the design of integrated circuits and was acceptable in the past because power circuits used to be operated at small switching frequencies. Therefore, the detailed switching characteristics of the active power semiconductor devices were of second-order importance, and the tradeoffs in the power circuit design were dominated to a large extent by capacitances and inductances. The situation has changed as applications tend to move to power circuits operated at higher switching frequencies. From this trend, the opportunities of reduced power losses and reduced sizes for the complete power system result. Moreover, international competition is forcing companies to speed up introduction of new products in the different applications fields of power electronic circuits without sacrificing product quality and reliability. The best way to take advantage of those opportunities to increase product innovation, reduce prototyping, and cope with economical pressure is, of course, to employ a CAD methodology, which accurately predicts the functionality and reliability of a specific power circuit design. This again means that high-quality power semiconductor device models for circuit simulation are required.

The trends and requirements for an upgrade of the CAD methodology for power circuit design as well as the necessity of improved power semiconductor device models for circuit simulation have not only been recognized on the academic side, but by the software industry too. A few specialized software vendors (like Analogy, Anacad, Mentor, Meta-Software, MicroSim, and Intusoft) have already reacted to these market opportunities and are offering enhanced support for the design of power electronic circuits. This includes also improved power device models incorporating many of the recent advances of the ongoing research. In fact, the software vendors are participating to some extent in these research activities on power device models for circuit simulation and pushing them ahead. In this paper, we will not discuss in detail the different models, which each of the vendors is offering, but restrict ourselves to the basic problems of modeling power semiconductor devices for circuit simulation and the status of

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TABLE I
RELEVANCE OF BASIC PHYSICAL PHENOMENA FOR DIFFERENT POWER DEVICES (++ VERY IMPORTANT, + IMPORTANT, 0 TO BE INCLUDED, - LESS IMPORTANT, - - NOT APPLICABLE)

	Diode	BJT	Thyristor/GTO	MOSFET	IGBT, MCT
Resistivity Modulation	++	++	++	++	++
Charge Storage	++	++	++	-	++
MOS-Capacitances	- -	- -	- -	++	++
Electro-Thermal	+	+	+	+	+
Breakdown	0	0	+	0	0

the research efforts for overcoming these problems. However, the reader can be sure that software companies are eager to incorporate these research advances into their products and that he will be able to get CAD support for his practical design problems, which reflects the current state of the art.

In the following sections, we will first (Section II) give an overview of the basic problems, which have to be overcome in the development phase of a useful circuit simulation model for a power semiconductor device. We will then (Section III) concentrate on the various attempts and ideas applied in the past to solve these basic problems and group them into categories of similar modeling concepts. Emphasis is put on the new concepts, introduced in recent years, which helped to advance the state of the art significantly. The subject of the subsequent section (Section IV) is the issue of parameter definition and determination, which emerges as one of the crucial remaining challenges for achieving a wide acceptance and application of the intended upgrade in the CAD methodology for the design of power electronic circuits. On the basis of the material presented and discussed, we then try (Section V) to give a comparison and relative evaluation of the known modeling concepts and finally (Section VI) discuss especially the possible trends of further future development and improvement of the present state of the art. It is of course unavoidable that these last two sections will reflect to some extent personal views and opinions of the authors.

II. BASIC PHYSICAL PHENOMENA AND MODELING PROBLEMS

For the development of power semiconductor device models, several effects have to be considered with high priority since they dominate the static and dynamic device characteristics. These effects are not described correctly by standard device models (or they are not included at all) because their influence on low-power devices is less important or neglectable. An accurate description, however, is essential for power devices.

Table I gives an overview of the main effects and their importance for the different power devices.

Modeling of these effects is based on one-dimensional (1-D) calculations in most cases. The majority of power semiconductor devices, however, have a structure with distinct two-dimensional (2-D) or three-dimensional (3-D) features, and, therefore, the 1-D idealization can be insufficient to describe the effects accurately. But more dimensional calculations increase the difficulty and complexity of finding solutions by such a drastic amount that they are applied only exceptionally.

A. Resistivity Modulation

To sustain high blocking voltages, power semiconductor devices have a thick lightly doped semiconductor layer. The resistance of this region determines the voltage drop and power loss when the device is in its conduction mode. This resistance is variable and its dependence on voltage or current can be highly nonlinear. In unipolar devices (MOSFET), the variations are caused by variations of the effective current-conducting area and by the mobility degradation with an increasing electric field. In bipolar devices [diode, bipolar junction transistor (BJT), thyristor, gate turn-off thyristor (GTO), insulated gate bipolar transistor (IGBT), and MOS-controlled thyristor (MCT)], the low-doped layer is swamped by electrons and holes when the device is in its on state. The density of the injected charge carriers can be much higher than the level of the doping concentration, and the resistivity of the region is significantly reduced.

The resistance of a region with the boundaries x_1 and x_r and the area A is given by

$$R = \int_{x_l}^{x_r} \frac{dx}{qA(\mu_n n + \mu_p p)} \tag{1}$$

where n and p are the densities of electrons and holes, respectively, and μ_n and μ_p are the mobilities of the charge carriers. In most cases, the charge carriers are not distributed homogeneously, and their density depends on position, and in some cases, the mobilities also cannot be regarded as constants. During transient operation, the variation of the resistivity does not follow the changing current instantaneously—this effect can influence the switching behavior (e.g., forward recovery of power diodes), and in order to take it into account, a dynamic description of the charge distribution is necessary. Even if a solution of the time-dependent charge densities is found, the calculation of the resistance remains difficult since the integration in (1) is not possible without simplifications.

B. Charge Storage

The charge carriers, which are stored in the lightly doped region of bipolar devices during the conduction mode, must be

extracted before the device can reach its blocking state. This effect causes switching delays and switching energy losses. Standard device models for circuit simulation use a quasi-static description of the charge carriers. It means that the charge distribution is always a function of the instantaneous voltages at the device terminals. This method is completely insufficient for power devices. A real dynamic description derived from the basic physical equations is required instead.

The charge stored in a low-doped region of a power device varies, under transient operation, with both time and position. This variation is determined by the ambipolar diffusion equation

$$\frac{dp}{dt} = -\frac{p}{\tau} + D\frac{d^2p}{dx^2} \tag{2}$$

where $p(x,t)$ is the density of the charge carriers, τ is the charge carrier lifetime, and D is the diffusion coefficient. This equation is valid in the case of high-level injection when hole and electron densities are approximately equal.

The slope of the charge carrier distribution is related to the currents—this relation is described by the transport equation

$$I = \left(1 + \frac{\mu_p}{\mu_n}\right)\left(I_n - qAD\frac{dp}{dx}\right) \tag{3}$$

where I_n is the electron current and I is the total current, the sum of electron and hole current. The integral of (2) together with the condition of (3) yields the charge control equation

$$\frac{dQ}{dt} = -\frac{Q}{\tau} + I_n(x_r) - I_n(x_l) \tag{4}$$

where x_r and x_l are the boundaries of the considered region and Q is the charge in this region.

One current component at each border is determined by the neighboring region. The total current is then obtained with (3), but this requires a solution of (2). Unfortunately, an exact analytical solution is not possible in the general case.

C. MOS Capacitances

Devices with isolated gate (MOSFET, IGBT, and MCT) have large capacitances which vary strongly with voltage in the different regions of operation. The capacitance of greatest importance is that between anode and gate. These are normally the output and input terminals of the device, and the resulting feedback has a dominating influence on the switching behavior. The capacitor is formed by the metal–oxide–semiconductor (MOS) structure resulting from the isolation of the gate from the semiconductor region. The value of the gate-anode capacitance C_{GA} can be calculated from the gate charge Q_G

$$C_{GA} = \frac{dQ_G}{dV_{GA}} = C_{ox}\frac{dV_{ox}}{dV_{GA}} \tag{5}$$

where C_{ox} is the capacitance of the plate capacitor which is determined by oxide thickness and area of the structure. The voltage V_{ox} across the oxide is a highly nonlinear function of the gate-anode voltage V_{GA} since at the surface of the semiconductor, below the gate, different states of the charge are possible. These states are called accumulation, depletion and inversion. Depending on the state, the derivative in (5) can vary between one and zero. Solutions of (5) are usually obtained with approximations treating the states separately, but this can lead to problems of abrupt changes in the capacitance or its derivative at transitions between different regimes of operation. Furthermore, dynamic transition states are possible.

D. Electrothermal Interaction

Due to high energy losses, power devices can heat up significantly during operation. The device characteristics depend strongly on the device temperature, therefore, the changing temperature influences the device behavior. To consider this interaction between thermal and electrical characteristics, electrothermal device models are required.

The device temperature T is calculated with the equation of heat transport

$$\frac{dT}{dt} = \frac{\lambda}{C'_{th}}\frac{d^2T}{dx^2} + \frac{P'}{C'_{th}} \tag{6}$$

where C'_{th} is the thermal capacitance per volume, λ is the thermal conductivity of the material, and P' is the generated thermal energy per volume. Thermal models usually use an average device temperature, which is then applied to the temperature-dependent parameters of the model equations. The temperature, however, is distributed inside the device and high temperature peaks can be localized in small regions.

E. Breakdown

Breakdown in power semiconductor devices occurs not only in the case of failure; in many applications breakdown happens during regular operation of the device (e.g., at turn off of GTO's). The most common breakdown mechanism is the avalanche effect due to impact ionization, but Zener breakdown and punchthrough are also possible.

The current increase due to the generation of charge carriers by impact ionization can be expressed by a multiplication factor M_p

$$I_p(w) = M_p I_p(0) = \frac{I_p(0)}{1 - \int \alpha_p \exp\int(\alpha_n - \alpha_p)\,dx'\,dx} \tag{7}$$

where α_n and α_p are ionization coefficients which depend on the electric field $E(x)$

$$\alpha_p = a_p \exp\left(-\frac{b_p}{E(x)}\right) \quad \alpha_n = a_n \exp\left(-\frac{b_n}{E(x)}\right).$$

The integral in (7) cannot be solved analytically since the electrical field is not constant. Furthermore, there is a feedback of the generated charge carriers on the electric field and during transient operation, the onset of the avalanche breakdown can be shifted significantly by the current flowing through the high-field region (dynamic avalanche). Usually, however, a constant breakdown voltage is used to model breakdown.

III. Modeling Concepts

To obtain models for the purpose of circuit simulations, relatively compact descriptions of the relevant effects must be

TABLE II
MODELING OF BASIC PHYSICAL PHENOMENA WITH DIFFERENT APPROACHES (+ APPLIED, 0 POSSIBLE, - NOT APPLICABLE)

	Functional Model	Approximate Solution	Transformation	Lumped Model	Numerical Solution
Resistivity Modulation	+	+	o	+	+
Charge Storage	+	+	+	+	+
MOS-Capacitances	+	+	-	+	o
Electro-Thermal	+	+	+	+	+
Breakdown	+	+	-	-	o

found because of practical restrictions in computing power. These descriptions must furthermore be implemented in the programs for circuit simulation.

The implementation occurs mainly in two ways: by so-called subcircuits or by mathematical functions. Mixed forms are also possible.

Subcircuit models are constructed by using conventional models which are available in the circuit simulation program and by combining them with passive components, switches, and controlled voltage and current sources. This method can lead to very complex and time-consuming models, and it is therefore mainly used if the simulation program does not provide the possibility to implement mathematical functions.

The much more efficient way is the insertion of model equations into the simulation program. However, this requires the respective capabilities to be available.

In most cases, it is not possible to obtain exact analytical solutions of the physical semiconductor equations, which are used as the basis [e.g., (1)–(7)]. Therefore, other methods must be used for the derivation of model equations. A large variety of approaches can be distinguished. Table II shows the most important methods and their applications to the different effects.

To explain the underlying ideas of the different approaches the example of charge storage is used. Modeling this effect can be regarded as the most challenging task in the construction of power semiconductor device models for circuit simulation.

A. Functional Model

The approach of a functional model treats the device as a "black box" and describes the externally observed behavior without a detailed consideration of the physical effects occurring inside the device [3]–[40].

1) Standard Low-Power Device Model: The standard low-power device models, which are available in circuit simulators, are adapted to power semiconductor devices by optimizing their parameters. Thereby, the parameters and model equations can lose their physical meaning, and a pure functional description may result. These models, however, are hardly able to simulate any high-voltage phenomena.

2) Lookup Table: In lookup tables, the data resulting directly from measurements or from calculations are stored and retrieved for simulation [18]. This method is well suited for DC characteristics, but it is much more difficult to use it for dynamic effects of the device in the environment of different circuits. The transient behavior of power semiconductor devices can depend on a large number of conditions which result from the state of the device before switching and the interactions of the device with other circuit elements during switching. Therefore, the effort becomes very large to consider all the situations caused by the varying conditions in many different circuit topologies.

3) Empirical Expressions: The equations of functional models are not obtained by rigorous derivations from the device physics. In many cases, they are selected arbitrary mathematical expressions which describe the externally observed behavior in a simplified way. But considerations of physical effects within the device can also be taken into account. If it is possible, the currents and voltages of the device terminals are approximated directly by straightforward functions. For a description of dynamic effects, however, it is often necessary to include additional variables into the equation set. These variables can be (but are not restricted to) internal variables of the device, e.g., the device charge. The relations between them and the external current and voltage waveforms are described by mathematical functions which are mainly obtained by intuitive assumptions. (These assumptions can be inspired by device physics, and, in some cases, they can be confirmed by theoretical derivations.) For example, the relation

$$Q(t) = -I(t)\tau_R \tag{8}$$

is used to approximate the reverse recovery of power diodes. τ_R is a time constant which determines how fast the turn-off reverse current of the diode decreases. A solution for the current is obtained with this relation and the simplified charge control equation (the difference of the electron currents is replaced by the total current). This solution, however, is valid only for the phase of turn off when the current decreases from its reverse peak to zero. Other switching phases must be described by other functions, and the solutions of the different phases must be adjusted to guarantee continuity.

B. Approximate Solution

The model equations of this approach are based on the device physics, but since exact solutions are not possible or restricted to a few special cases, appropriate mathematical representations are found to approximate the solution [41]–[115].