

**THE OPEN UNIVERSITY OF SRI LANKA
BACHELOR OF TECHNOLOGY - LEVEL 5
ECX5236 – COMPUTER ARCHITECTURE
FINAL EXAMINATION 2011**



DURATION : THREE HOURS

DATE : 19th March 2012

TIME : 1400 - 1700 HOURS

Answer any *five* questions. All questions carry equal marks.

1.

- (i) Describe the two methods, namely hardwired and microprogrammed control, in designing the Control Unit of a computer.
- (ii) The hardwired control design of a Control Unit can be accomplished in 5 steps. Briefly explain those steps.
- (iii) Describe and distinguish between vertical microinstructions and horizontal microinstructions.
- (iv) In order to evaluate the cost of each design, microprogrammed or the hardwired control we can use the chip area required for each design. In a particular design microprogramming has a fixed cost of 1000 units of chip area and a variable cost of 1 unit of chip area for the ROM to store each microinstruction. Hardwired control has a cost of 5 units of chip for each instruction. When will the microprogrammed control method be more economical?

2.

- (i) Briefly describe Very Long Instruction Word (VLIW) approach of Multiple-issue processors.
- (ii) What are the advantages and disadvantages of a Superscalar implementation and a VLIW approach?
- (iii) Compare single component and multi component addressing modes.
- (iv) What are the addressing modes of the following Intel 8086 instructions?
 - (a) MOV AL, BL ; (AL) \leftarrow (BL)
 - (b) ADD AL, data ; (AL) \leftarrow (AL) + data
 - (c) AND AX, addr ; (AX) \leftarrow (AX) AND (addr)

Note : AL, AX and BL belong to the register set. Here *addr* is an address of a memory location and *data* is a data value.

3.

- (i) Describe the Flynn's classification (SISD, SIMD, MISD and MIMD) on computer organisation giving block diagrams for each organization.
- (ii) Distinguish MIMD multiprocessors from multi-computers or computer networks.

- (iii) What are the salient features of RISC architecture and CISC architecture? Provide advantages and disadvantages of each architecture.
- (iv) A processor executes 10 million floating point and one million overhead instructions in 50 ms. What is the MFLOPS rating of this processor? What would be the MIPS rating of the same processor?
- 4.
- (i) Throughput of a pipeline is inversely proportional to the bottleneck of the pipeline. Explain the statement.
- (ii) An instruction execution path will take 9ns to execute an instruction in one-stage pipeline. However this logic path can be divided into any number of stages and the logic delay (9ns) can be subdivided equally as well. Moreover the sum of setup time of a latch and clock skew will be 1ns. Let s as the number of stages. Assume that the pipeline receives a set of instructions without branching instructions.
- (a) What is the clock period T_{clock} in terms of s ?
- (b) What is the execution time of 101 instructions?
- (c) Calculate the optimum number of stages that the pipeline should have for minimum execution time of 101 instructions.
- 5.
- (i) What is meant by a page fault in virtual memory organization?
- (ii) When a page fault occurs describe what the computer system would do.
- (iii) A disk subsystem employed for the virtual memory organization has the following specifications: 32 sectors per track, 512 bytes per sector, 3600 rpm, average linear latency of 30 ms, page size of 4 Kbytes. In average the computer system executes an instruction in 1.5 μ s.
- (a) Calculate the data transfer rate of the disk subsystem.
- (b) Compute the wasted time in the event of a page fault while executing a program.
- (c) What should be the seek time of the disk drive in order to reduce the wasted time, to less than 85%?
6. A simple analogue to digital converter (SADC) is interfaced to a PC via parallel port (Appendix A) or ISA bus (Appendix B) to measure analogue signals. SADC operates as follows.
- When the PC sets the SOC (Start of Conversion) signal then SADC reads the input analogue signal and starts the conversion. After completing the conversion, SADC sets the interrupt signal EOC (End of Conversion) which will be sent to PC to indicate the end of the operation.
- Digital equivalent (D) of analogue signal is inversely proportional to the time (T seconds) between SOC and EOC signals. Hence, digital equivalent can be computed as $D = 2K/T$ (where "K" is a predefined constant), and the width is 8 bits.

- (i) Draw a block diagram to show the connectivity of the device with the computer through the parallel port (Appendix A) or ISA bus (Appendix B). Clearly indicate address, data and control signals that involve and the pins of parallel port or ISA Bus.
 - (ii) Draw a typical timing diagram for reading data from the SADC.
 - (iii) Give an algorithm to compute digital equivalent. You must show all value used for configuring the ISA bus (data and address) or the parallel port (data and address of relevant ports).
 - (iv) Explain how to use a Logic Analyzer for timing analysis with the help of your block diagram. Clearly indicate address, data and control signals that involve and the pins of parallel port or ISA Bus.
7. An enhancement in a computer system improves only some part of the system. Accordingly improvement of the performance depends on the impact of the enhanced part. The f denotes the fraction of the computation time in the old system that can be improved with the enhancement made; S_e is the achievable speedup only if the enhanced part of the system is used.
- (i) If the old time of the system (without improvement) is T_{old} formulate the new time T_{new} of the system after the enhancement.
 - (ii) The speedup of the new system (after the improvement) is

$$S_{new} = \frac{T_{old}}{T_{new}}.$$

Accordingly derive the Amdahl's law in terms of f , S_e , S_{new} .
 - (iii) Restate this law for multiprocessor system, where f is the fraction of the computation time which is parallelizable, n is the number of processors in the system.
 - (iv) Initially multiprocessor system has 8 processors. To improve the system it is decided to double the number of processors. What would be the minimum fraction of parallelizable part of an application that increases the speedup by more than 1.7 times of the old system?
- 8.
- (i) Write policies are needed for data caches when an instruction writes data to the cache. Briefly describe the Write Back and Write Through policies.
 - (ii) A hierarchical Cache – Main Storage memory subsystem has following specifications: cache access time of 50ns, main storage access time of 500ns, 80% of memory request are for read, hit ratio of 0.9 for read access and the Write Through policy is employed. Estimate the following.
 - (a) Average access time of the system considering only the memory read cycle.
 - (b) Average access time of the system both for read and write requests.
 - (c) The hit ratio taking into consideration the write cycle.

Appendix A

Parallel port connector description

Pin: D-sub	Signal	Function	Source	Register		Inverted at con- nector?	Pin: Centron -ics
				Name	Bit #		
1	nStrobe	Strobe D0-D7	PC ¹	Control	0	Y	1
2	D0	Data Bit 0	PC ²	Data	0	N	2
3	D1	Data Bit 1	PC ²	Data	1	N	3
4	D2	Data Bit 2	PC ²	Data	2	N	4
5	D3	Data Bit 3	PC ²	Data	3	N	5
6	D4	Data Bit 4	PC ²	Data	4	N	6
7	D5	Data Bit 5	PC ²	Data	5	N	7
8	D6	Data Bit 6	PC ²	Data	6	N	8
9	D7	Data Bit 7	PC ²	Data	7	N	9
10	nAck	Acknowledge (may trigger interrupt)	Printer	Status	6	N	10
11	Busy	Printer busy	Printer	Status	7	Y	11
12	PaperEnd	Paper end, empty (out of paper)	Printer	Status	5	N	12
13	Select	Printer selected (on line)	Printer	Status	4	N	13
14	nAutoLF	Generate automatic line feeds after carriage returns	PC ¹	Control	1	Y	14
15	nError (nFault)	Error	Printer	Status	3	N	32
16	nInit	Initialize printer (Reset)	PC ¹	Control	2	N	31
17	nSelectIn	Select printer (Place on line)	PC ¹	Control	3	Y	36
18	Gnd	Ground return for nStrobe, D0					19,20
19	Gnd	Ground return for D1, D2					21,22
20	Gnd	Ground return for D3, D4					23,24
21	Gnd	Ground return for D5, D6					25,26
22	Gnd	Ground return for D7, nAck					27,28
23	Gnd	Ground return for nSelectIn					33
24	Gnd	Ground return for Busy					29
25	Gnd	Ground return for nInit					30
	Chassis	Chassis ground					17
	NC	No connection					15,18,34
	NC	Signal ground					16
	NC	+5V	Printer				35

¹Setting this bit high allows it to be used as an input (SPP only)²Some Data ports are bidirectional.

Parallel port register definitions

Base address: 0378h

Data Register (Base Address)

<i>Bit</i>	<i>Pin: D-sub</i>	<i>Signal Name</i>	<i>Source</i>	<i>Inverted at connector?</i>	<i>Pin: Centronics</i>
0	2	Data bit 0	PC	no	2
1	3	Data bit 1	PC	no	3
2	4	Data bit 2	PC	no	4
3	5	Data bit 3	PC	no	5
4	6	Data bit 4	PC	no	6
5	7	Data bit 5	PC	no	7
6	8	Data bit 6	PC	no	8
7	9	Data bit 7	PC	no	9

Some Data ports are bidirectional. (See Control register, bit 5 below.)

Status Register (Base Address +1)

<i>Bit</i>	<i>Pin: D-sub</i>	<i>Signal Name</i>	<i>Source</i>	<i>Inverted at connector?</i>	<i>Pin: Centronics</i>
3	15	nError (nFault)	Peripheral	no	32
4	13	Select	Peripheral	no	13
5	12	PaperEnd	Peripheral	no	12
6	10	nAck	Peripheral	no	10
7	11	Busy	Peripheral	yes	11

Additional bits not available at the connector:

0: may indicate timeout (1=timeout).

1, 2: unused

Control Register (Base Address +2)

<i>Bit</i>	<i>Pin: D-sub</i>	<i>Signal Name</i>	<i>Source</i>	<i>Inverted at connector?</i>	<i>Pin: Centronics</i>
0	1	nStrobe	PC ¹	yes	1
1	14	nAutoLF	PC ¹	yes	14
2	16	nInit	PC ¹	no	31
3	17	nSelectIn	PC ¹	yes	36

¹When high, PC can read external input (SPP only).

Additional bits not available at the connector:

4: Interrupt enable. 1=IRQs pass from nAck to system's interrupt controller. 0=IRQs do not pass to interrupt controller.

5: Direction control for bidirectional Data ports. 0=outputs enabled. 1=outputs disabled; Data port can read external logic voltages.

6,7: unused

Appendix B

ISA (Industry Standard Architecture) Bus

Pins layout

D	Description	Name	Pin	Pin	Name	Description	D
/	Ground	GND	B1	A1	IO CHK	I/O Channel Check	-I
O	Reset	RESET	B2	A2	SD7	System Data bit 7	I/O
/	Power +5V	+5V	B3	A3	SD6	System Data bit 6	I/O
I	Interrupt Request 9	IRQ9	B4	A4	SD5	System Data bit 5	I/O
/	Power -5V	-5V	B5	A5	SD4	System Data bit 4	I/O
I	DMA Request 2	DRQ2	B6	A6	SD3	System Data bit 3	I/O
/	Power -12V	-12V	B7	A7	SD2	System Data bit 2	I/O
/	Zero Wait State	0WS	B8	A8	SD1	System Data bit 1	I/O
/	Power +12V	+12V	B9	A9	SD0	System Data bit 0	I/O
/	Ground	GND	B10	A10	IO RDY	I/O Channel Ready	-I
O	System Memory Write	SMEMW	B11	A11	AEN	Address Enable	O
O	System Memory Read	SMEMR	B12	A12	SA19	System Address bit 19	O
I/O	I/O Write	IOW	B13	A13	SA18	System Address bit 18	O
I/O	I/O Read	IOR	B14	A14	SA17	System Address bit 17	O
O	DMA Request Acknowledge 3	DACK3	B15	A15	SA16	System Address bit 16	O
I	DMA Request 3	DRQ3	B16	A16	SA15	System Address bit 15	O
O	DMA Request Acknowledge 1	DACK1	B17	A17	SA14	System Address bit 14	O
I	DMA Request 1	DRQ1	B18	A18	SA13	System Address bit 13	O
I/O	Refresh cycle in progress	REFRESH	B19	A19	SA12	System Address bit 12	O
O	System Clock	CLOCK	B20	A20	SA11	System Address bit 11	O
I	Interrupt Request 7	IRQ7	B21	A21	SA10	System Address bit 10	O
I	Interrupt Request 6	IRQ6	B22	A22	SA9	System Address bit 9	O
I	Interrupt Request 5	IRQ5	B23	A23	SA8	System Address bit 8	O
I	Interrupt Request 4	IRQ4	B24	A24	SA7	System Address bit 7	O
I	Interrupt Request 3	IRQ3	B25	A25	SA6	System Address bit 6	O
O	DMA Request Acknowledge 2	DACK2	B26	A26	SA5	System Address bit 5	O
O	T/C	TC	B27	A27	SA4	System Address bit 4	O
?	Buffered Address Latch Enable	BALE	B28	A28	SA3	System Address bit 3	O
/	Power +5V	+5V	B29	A29	SA2	System Address bit 2	O
O	Oscillator	OSC	B30	A30	SA1	System Address bit 1	O
/	Ground	GND	B31	A31	SA0	System Address bit 0	O

Signal Description

CLOCK (System Drive) output

The system clock is a synchronous microprocessor cycle clock.

RESET (Reset Drive) output

This signal goes high at power-up, hardware reset, or when low line-voltage occurs.

SA0 to SA19 (System Addresses) input/output

The system address lines run from bit 0 through 19. They are latched onto the falling edge of BALE.

SD0 to SD7 (System Data bits) Input/Output

System data bits 0 to 7.

BALE (*Buffered Address Latch Enable*) input

The buffered address latch enable is used in latch SA0 to SA19 on the falling edge of BALE. During DMA cycles, BALE is forced high.

IO CHK (*I/O Channel Check*) active low input

I/O channel check is active low signal which indicate that a parity error exists in the I/O board.

IO RDY (*I/O Channel Ready*) input

This signal lengthens I/O or memory cycles and should be held low with valid addresses. It can be held low for a maximum of 2.5 microseconds.

IRQ 3 to 7, 9 (*Interrupt Requests*) input

These interrupt request signals indicate I/O service request attention. They are prioritized in the following sequences: highest IRQ 9 and lowest IRQ 3, 4, 5, 6, 7, 8.

IOR (*I/O Read*) active low input/output

Instructs an I/O device to drive its data onto the data bus.

IOW (*I/O Write*) active low output

Instructs an I/O device to read the data off the data bus.

SMEMR (*System Memory Read*) output

The system memory read signal is low while the low first megabyte memory is being read.

SMEMW (*System Memory Write*) output

The system memory write signal is low while the low first megabyte memory is being written.

DRQ 0 to 3 (*DMA Requests*) active high input

DMA Request channels 0 to 3 are for 8-bit data transfers. DRQ4 is used on the system board. Hold a DRQ line high until its DMA Request Acknowledge (DACK) goes active. Their priority is in the following sequences: highest DRQ 0, 1, 2, and 3.

DACK 1 to 3 (*DMA Request Acknowledges*) output

These signals are used to acknowledge the corresponding signals for DRQ 0 to 3.

AEN (*Address Enable*) output

The address enable is high when the DMA controller drives the address bus and is low when the CPU drives the address bus.

REFRESH (*Refresh cycle in progress*) active low input/output

This signal indicates a refresh cycle is in progress.

TC (*T/C*) output**OSC** (*Oscillator*) output

The oscillator signal is used for the color graphic card.
High-speed clock (70 ns, 14.31818 MHz), 50% duty cycle

OWS (*Zero Wait State*) input

The zero wait state indicates to the microprocessor that the present bus cycle can be completed without inserting any additional wait cycles.