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The Open University of Sri Lanka
Faculty of Engineering Technology

Study Programme	:	Bachelor of Technology (Engineering)
Name of the Examination	:	Final Examination
Course Code and Title	**:**	**MEX5270 Power electronics and motor drives**
Academic Year	:	2012/2013
Date	:	10th August 2013
Time	:	9.30am – 12.30pm
Duration	:	3 hours

General instructions

1. Read all instructions carefully before answering the questions.
2. This question paper consists of 8 questions. All questions carry equal marks.
3. Answer any 5 questions only.

Q1.

a. Discuss *Conduction loss* and *Switching loss* of real power semiconductor switches using appropriate diagrams.
b. Briefly describe *four quadrant dc drives* and their functionalities.
c. Discuss the principle of regenerative breaking of dc – dc converter fed dc motor drives.
d. A full bridge inverter produces a 200V square wave at 50Hz across a series R-L load where R=10 Ω and L=50mH. The relevant waveforms are shown in Figure Q1. Find the following
   i. An expression of load current in positive half cycle and negative half cycle
   ii. Peak value of the load current

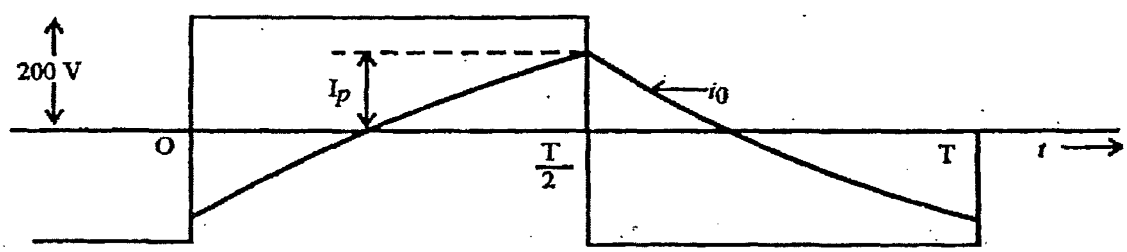

Figure Q1

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Q2. A transistor with a snubber circuit experiences a liner fall in current from 50A to 0A in 1.5μs at turn-off. At turn-on the transistor experiences a linear fall in voltage from its off state value of 200V to 0V in 1.2μs.

Determine the following if the voltage rise time is delayed to 0.5μs, 1.0μs and 1.5μs.

i. Value of the capacitor
ii. Transistor switching loss during turn-off
iii. Capacitor stored energy
iv. Total loss

Observing the results you obtained, suggest a suitable value for the snubber resistance, if $t_{on(min)}$= 10μs. Give reasons for your answer.

Q3.

a) The turn ON and the turn OFF switching transition times for the power semiconductor switch S in Figure Q3(a) are respectively $t_{sw(on)}$ and $t_{sw(off)}$. Assume linear variation of current and voltage during the switching transitions. The ON state voltage drop across the switch is V_D.

Show that the average switching power loss across the switch is

$$P_{SW} = \left(\frac{VI}{6} + \frac{V_D I}{3}\right)\left(t_{SW(on)} + t_{SW(off)}\right) f_S$$

Where V is the off state voltage across the switch, I is the ON state current through the switch and f_S is the switching frequency.

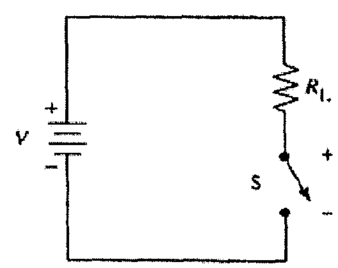

Figure Q3(a)

b) Consider the single phase controlled half wave bridge rectifier shown in Figure Q3(b). The firing delay angle is 45^0. Draw the waveforms of the half wave bridge rectifier for the following clearly labeling the graphs.

i. Supply voltage (v_s)
ii. Output voltage (v_o)
iii. Output current (i)
iv. Voltage across the SCR (v_{SCR})

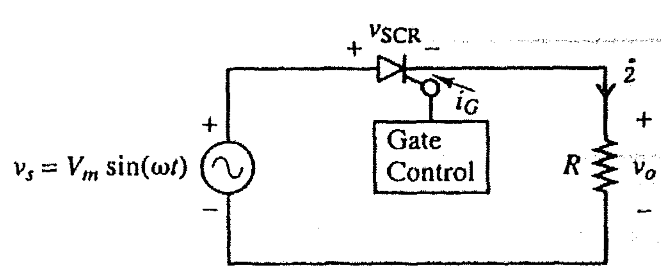

Figure Q3(b)

Q4.

a) Compare and contrast controlled and uncontrolled rectification.

b) The single phase full bridge rectifier shown below has an AC source with V_m=100V at 60Hz and a series R-L load with R_L=10Ω and L= 10mH.

Determine

i. the average current in the load
ii. the power absorbed by the load
iii. the average and rms current in the diode.

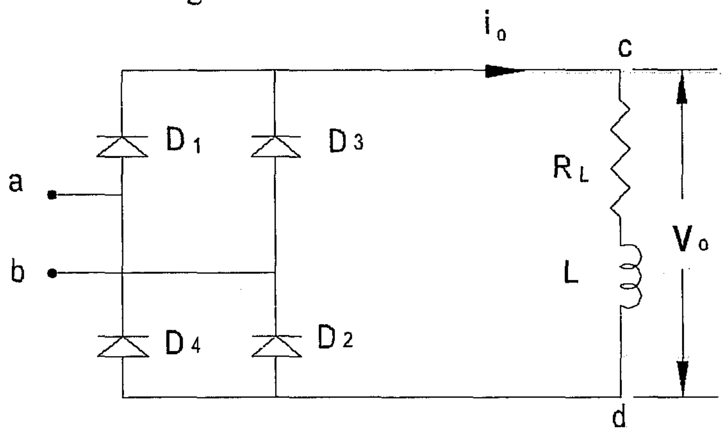

Figure Q4

Q5. The single phase AC voltage controller of Figure Q5(a) has a 120V_{rms} 60Hz source and a load resistance of 15Ω. The delay angle α is 90^0.

a. Draw the wave forms of v_s, i_o, v_o and v_{sw} (the voltage across the SCRs)
Note:- Use three graphs. v_s and i_o on one graph and others on separate graphs.

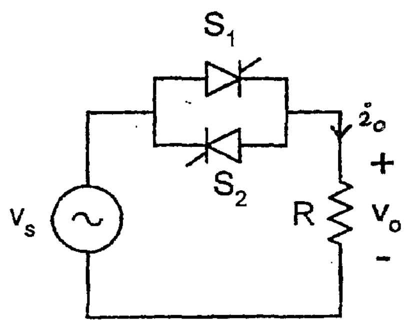

Figure Q5(a)

b. Determine the following

i. the rms load voltage
ii. the power absorbed by the load
iii. the power factor
iv. the rms and average currents in the SCRs

NOTE:- Use the graph given in Figure Q5(b) as applicable

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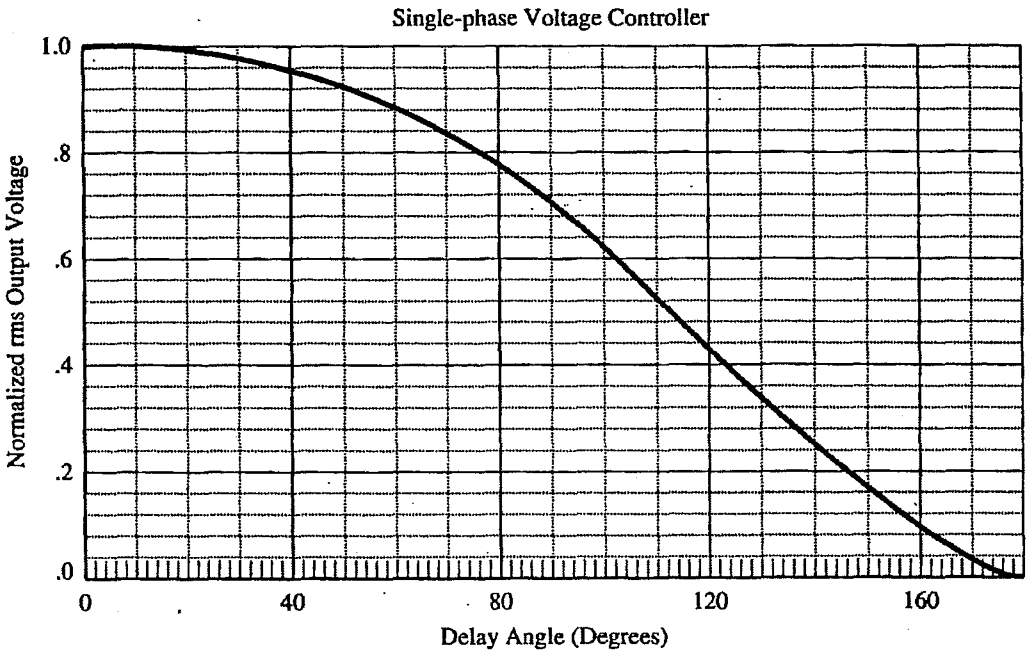

Figure Q5(b) The Normalized rms load voltage versus delay angle for a single phase ac voltage controller with a resistive load

Q6. A buck converter has an input voltage , V_d=15V. The required average output voltage V_o = 5V and the peak to peak output ripple voltage is 10mV. The switching frequency is 20KHz. The peak to peak ripple current of the inductor is limited to 1A. Determine

i. the duty cycle D
ii. the filter inductor L
iii. the filter capacitor C

Q7. The buck boost converter as shown in Figure Q7 has V_d= 24V, V_o=36V and a load resistance of 10Ω. The switching frequency of the converter is 60kHz.

i. Determine the inductance value such that the minimum inductor current is 40% of its average value.
ii. Determine the capacitance required to limit the output voltage ripple to 0.5%.

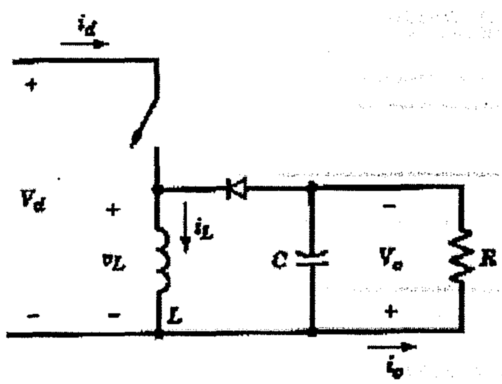

Figure Q7

Q8. A full bridge inverter is used to produce a 60Hz voltage across a series R-L load using bipolar PWM. The dc input to the bridge is 100V, the amplitude modulation ratio m_a is 0.8, and the frequency modulation ratio m_f is 21. The load has a resistance R = 10Ω and inductance L = 20mH.

Determine the following

i. The amplitude of the 60Hz component of the output voltage and load current

ii. The power absorbed by the load resistance

NOTE:- Use the values given in Table Q8 as applicable

	$M_a = 1$	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2	0.1
$n = 1$	1.00	0.90	0.80	0.70	0.60	0.50	0.40	0.30	0.20	0.10
$n = m_f$	0.60	0.71	0.82	0.92	1.01	1.08	1.15	1.20	1.24	1.27
$n = m_f \pm 1$	0.32	0.27	0.22	0.17	0.13	0.09	0.06	0.03	0.02	0.00

Table Q8 Normalized Fourier coefficients $\frac{V_n}{V_{dc}}$ for bipolar PWM

END