**THE OPEN UNIVERSITY OF SRI LANKA**
**BACHELOR OF TECHNOLOGY - LEVEL 5**
**ECX5236 – COMPUTER ARCHITECTURE**
**FINAL EXAMINATION 2012**

**DURATION : THREE HOURS**

**DATE : 19th August 2013** **TIME : 0930 - 1230 HOURS**

Answer any ***five*** questions. All questions carry equal marks.

1.

(i) Draw typical virtual machine schematics for different styles of Instruction Set Architecture (ISA) i.e. Accumulator, Memory-Memory, Stack, Load-Store.

(ii) A processor based on Load-Store architecture is designed with the following specifications. The basic minimum requirement is identified as 1M word memory, 32 instructions with 4 different addressing modes. An option of register operand with 32 CPU registers has been also proposed.

(a) What should be the instruction formats with the register operand option?

(b) What should be the instruction formats without the register operand option?

(c) Specify the details of each instruction type and operation code which should be supported on the design.

(d) Draw a block diagram for the processor including all necessary components.

2.

(i) Briefly describe the classes of pipeline hazards.

(ii) You are provided with a floating-point multiplier pipeline and a floating-point adder pipeline. Each pipeline has four segments. Multiplexers and registers are also provided.

(a) Show how you can design a pipeline processor for a quadric matrix multiplication. Draw a block diagram and describe it.
**Note:** if **A** and **B** are $n \times n$ matrices, the matrix multiplication will be **C**=**AB**, where **C** is $n \times n$ matrix. Each element $c_{ij}$ of matrix **C** can be calculated as follows:

$$c_{ij} = \sum_{k=1}^{n} a_{ik} \times b_{kj} ,$$

where i=1,2,...,n and j=1,2,...,n;
$a_{ik}$ , $b_{kj}$ - elements of matrices **A** and **B** respectively.

(b) Estimate the time taken for the multiplication of two 4x4 matrices.

3.

(i) Briefly describe the tasks of an I/O system of a computer.

(ii) Briefly describe the following I/O control systems: Programmed I/O, Interrupt I/O, and Coprocessor I/O.

(iii) A system has the following specifications: 500 ns memory cycle time for read/ write, average of 2μs for execution of an instruction. Determine the peak data transfer rate for

(a) Interrupt Driven IO, assuming interrupt service routine to be 7 instructions;

(b) Programmed IO, assuming each byte transfer requires 4 instructions.

4.

(i) Briefly describe what an instruction pipeline is.

(ii) An instruction execution path will take $T$ ns to execute an instruction in one-stage pipeline. However this logic path can be divided into any number of stages and the logic delay ($T$ ns) may be able to subdivide equally as well. Moreover the sum of setup time of a latch and clock skew will be $\tau$ ns. Let $k$ as the number of stages.

(a) What is the execution time of $n$ number of instructions in one-stage pipeline?

(b) What is the clock period $T_{clock}$ of the pipeline in terms of $T$, $k$ and $\tau$?

(c) What is the execution time of $n$ number of instructions in the multistage pipeline (with $k$ stages)?

(d) Derive an equation to find the minimum number of instructions (the smallest $n$) to have less execution time in a multistage pipeline than a one-stage pipeline.

(e) Using the above equation show that execution of only one instruction in a pipeline will decrease the performance.

5.

(i) What is meant by a page fault in virtual memory organization?

(ii) When a page fault occurs describe what the computer system would do.

(iii) For the virtual memory organization a hard disk is purchased for employing disk subsystem. According to the vendor the following specifications are given: 8 GB capacity, 1024 cylinders, 255 heads, 63 sectors, 7200 rpm and average seek time 9ms. The page size of the virtual memory is 8 Kbytes. Performance of the computer system is given as 100 MIPS

(a) Calculate the number of bytes in a sector of the hard disk. (Note: bytes in a sector should be the nearest to the power of two value)

(b) Calculate the data transfer rate of the disk subsystem.

(c) Compute the wasted time in the event of a page fault while executing a program.

6. You are to connect an external device, which sends sensor values as a 4 bit data to a computer through the parallel port or through the ISA bus. The device sets its *data valid* pin when it is ready to send data. As soon as the device receives *Data accepted* signal it resets *data valid* pin until the next data is ready.

(i) Draw a block diagram to show the connectivity of the device with the computer through the parallel port (Appendix A) or ISA bus (Appendix B). Indicate which pins of the parallel port or the ISA bus you are going to connect with the pins of the device.

(ii) Draw a typical timing diagram for reading data from the device.

(iii) Give an algorithm for receiving a 4 bit data from the device. You must show all values used for configuring the ISA bus (values for address bus and the data bus) or the parallel port (addresses and values of the relevant ports) each time when they are used.

(iv) Expand your algorithm to continuously receive data in a given period of time.

7. It is observed that in a computer system, memory operations take 40% of the execution time. Usually L1 cache speeds up 75% of the memory operations by 5 times and L2 cache can speed up only 60% of the rest of the memory operations by 3 times. Assume that sections of execution sped up by L1 and L2 caches do not overlap.

(i) Draw a diagram to illustrate the above scenario indicating the percentages/factors of each section of execution.

(ii) Calculate the speedup when the system has only L1 cache.

(iii) Calculate the achievable speedup when the system has both L1 and L2 caches.

(iv) Describe the working principle of cache memory.

8.

(i) Briefly describe the major objectives of a memory hierarchy.

(ii) Name three organizations of cache memory and describe them briefly.

(iii) Comment on the following statement giving reasons.

*"Hit ratio can be improved by using faster memory i.e. memory with less access time."*

(iv) A virtual memory system has memory access time of 500 ns, secondary storage access time of 20ms and average access time of 4.4ms.

(a) Compute the hit ratio for the virtual memory system.

(b) Describe two suitable hardware and/or software schemes to reduce the average access time.

**Appendix A**

## Parallel port connector description

| Pin: D-sub | Signal | Function | Source | Register | | Inverted at con-nector? | Pin: Centron -ics |
|---|---|---|---|---|---|---|---|
| | | | | Name | Bit # | | |
| 1 | nStrobe | Strobe D0-D7 | PC[1] | Control | 0 | Y | 1 |
| 2 | D0 | Data Bit 0 | PC[2] | Data | 0 | N | 2 |
| 3 | D1 | Data Bit 1 | PC[2] | Data | 1 | N | 3 |
| 4 | D2 | Data Bit 2 | PC[2] | Data | 2 | N | 4 |
| 5 | D3 | Data Bit 3 | PC[2] | Data | 3 | N | 5 |
| 6 | D4 | Data Bit 4 | PC[2] | Data | 4 | N | 6 |
| 7 | D5 | Data Bit 5 | PC[2] | Data | 5 | N | 7 |
| 8 | D6 | Data Bit 6 | PC[2] | Data | 6 | N | 8 |
| 9 | D7 | Data Bit 7 | PC[2] | Data | 7 | N | 9 |
| 10 | nAck | Acknowledge (may trigger interrupt) | Printer | Status | 6 | N | 10 |
| 11 | Busy | Printer busy | Printer | Status | 7 | Y | 11 |
| 12 | PaperEnd | Paper end, empty (out of paper) | Printer | Status | 5 | N | 12 |
| 13 | Select | Printer selected (on line) | Printer | Status | 4 | N | 13 |
| 14 | nAutoLF | Generate automatic line feeds after carriage returns | PC[1] | Control | 1 | Y | 14 |
| 15 | nError (nFault) | Error | Printer | Status | 3 | N | 32 |
| 16 | nInit | Initialize printer (Reset) | PC[1] | Control | 2 | N | 31 |
| 17 | nSelectIn | Select printer (Place on line) | PC[1] | Control | 3 | Y | 36 |
| 18 | Gnd | Ground return for nStrobe, D0 | | | | | 19,20 |
| 19 | Gnd | Ground return for D1, D2 | | | | | 21,22 |
| 20 | Gnd | Ground return for D3, D4 | | | | | 23,24 |
| 21 | Gnd | Ground return for D5, D6 | | | | | 25,26 |
| 22 | Gnd | Ground return for D7, nAck | | | | | 27,28 |
| 23 | Gnd | Ground return for nSelectIn | | | | | 33 |
| 24 | Gnd | Ground return for Busy | | | | | 29 |
| 25 | Gnd | Ground return for nInit | | | | | 30 |
| | Chassis | Chassis ground | | | | | 17 |
| | NC | No connection | | | | | 15,18,34 |
| | NC | Signal ground | | | | | 16 |
| | NC | +5V | Printer | | | | 35 |

[1]Setting this bit high allows it to be used as an input (SPP only)

[2]Some Data ports are bidirectional.

## Parallel port register definitions

**Base address:** 0378h

| **Data Register (Base Address)** | | | | | |
|---|---|---|---|---|---|
| ***Bit*** | ***Pin: D-sub*** | **Signal Name** | **Source** | **Inverted at connector?** | **Pin: Centronics** |
| 0 | 2 | Data bit 0 | PC | no | 2 |
| 1 | 3 | Data bit 1 | PC | no | 3 |
| 2 | 4 | Data bit 2 | PC | no | 4 |
| 3 | 5 | Data bit 3 | PC | no | 5 |
| 4 | 6 | Data bit 4 | PC | no | 6 |
| 5 | 7 | Data bit 5 | PC | no | 7 |
| 6 | 8 | Data bit 6 | PC | no | 8 |
| 7 | 9 | Data bit 7 | PC | no | 9 |
| Some Data ports are bidirectional. (See Control register, bit 5 below.) | | | | | |
| **Status Register (Base Address +1)** | | | | | |
| ***Bit*** | ***Pin: D-sub*** | **Signal Name** | **Source** | **Inverted at connector?** | **Pin: Centronics** |
| 3 | 15 | nError (nFault) | Peripheral | no | 32 |
| 4 | 13 | Select | Peripheral | no | 13 |
| 5 | 12 | PaperEnd | Peripheral | no | 12 |
| 6 | 10 | nAck | Peripheral | no | 10 |
| 7 | 11 | Busy | Peripheral | yes | 11 |
| Additional bits not available at the connector:<br>0: may indicate timeout (1=timeout).<br>1, 2: unused | | | | | |
| **Control Register (Base Address +2)** | | | | | |
| ***Bit*** | ***Pin: D-sub*** | **Signal Name** | **Source** | **Inverted at connector?** | **Pin: Centronics** |
| 0 | 1 | nStrobe | PC[1] | yes | 1 |
| 1 | 14 | nAutoLF | PC[1] | yes | 14 |
| 2 | 16 | nInit | PC[1] | no | 31 |
| 3 | 17 | nSelectIn | PC[1] | yes | 36 |
| [1]When high, PC can read external input (SPP only).<br>Additional bits not available at the connector:<br>4: Interrupt enable. 1=IRQs pass from *nAck* to system's interrupt controller. 0=IRQs do not pass to interrupt controller.<br>5: Direction control for bidirectional Data ports. 0=outputs enabled. 1=outputs disabled; Data port can read external logic voltages.<br>6,7: unused | | | | | |

## Appendix B

# ISA (Industry Standard Architecture) Bus

### Pins layout

| D | Description | Name | Pin | Pin | Name | Description | D |
|---|---|---|---|---|---|---|---|
| / | Ground | GND | B1 | A1 | IO CHK | I/O Channel Check | -I |
| O | Reset | RESET | B2 | A2 | SD7 | System Data bit 7 | I/O |
| / | Power +5V | +5V | B3 | A3 | SD6 | System Data bit 6 | I/O |
| I | Interrupt Request 9 | IRQ9 | B4 | A4 | SD5 | System Data bit 5 | I/O |
| / | Power -5V | -5V | B5 | A5 | SD4 | System Data bit 4 | I/O |
| I | DMA Request 2 | DRQ2 | B6 | A6 | SD3 | System Data bit 3 | I/O |
| / | Power -12V | -12V | B7 | A7 | SD2 | System Data bit 2 | I/O |
| / | Zero Wait State | 0WS | B8 | A8 | SD1 | System Data bit 1 | I/O |
| / | Power +12V | +12V | B9 | A9 | SD0 | System Data bit 0 | I/O |
| / | Ground | GND | B10 | A10 | IO RDY | I/0 Channel Ready | -I |
| O | System Memory Write | SMEMW | B11 | A11 | AEN | Address Enable | O |
| O | System Memory Read | SMEMR | B12 | A12 | SA19 | System Address bit 19 | O |
| I/O | I/O Write | IOW | B13 | A13 | SA18 | System Address bit 18 | O |
| I/O | I/O Read | IOR | B14 | A14 | SA17 | System Address bit 17 | O |
| O | DMA Request Acknowledge 3 | DACK3 | B15 | A15 | SA16 | System Address bit 16 | O |
| I | DMA Request 3 | DRQ3 | B16 | A16 | SA15 | System Address bit 15 | O |
| O | DMA Request Acknowledge 1 | DACK1 | B17 | A17 | SA14 | System Address bit 14 | O |
| I | DMA Request 1 | DRQ1 | B18 | A18 | SA13 | System Address bit 13 | O |
| I/O | Refresh cycle in progress | REFRESH | B19 | A19 | SA12 | System Address bit 12 | O |
| O | System Clock | CLOCK | B20 | A20 | SA11 | System Address bit 11 | O |
| I | Interrupt Request 7 | IRQ7 | B21 | A21 | SA10 | System Address bit 10 | O |
| I | Interrupt Request 6 | IRQ6 | B22 | A22 | SA9 | System Address bit 9 | O |
| I | Interrupt Request 5 | IRQ5 | B23 | A23 | SA8 | System Address bit 8 | O |
| I | Interrupt Request 4 | IRQ4 | B24 | A24 | SA7 | System Address bit 7 | O |
| I | Interrupt Request 3 | IRQ3 | B25 | A25 | SA6 | System Address bit 6 | O |
| O | DMA Request Acknowledge 2 | DACK2 | B26 | A26 | SA5 | System Address bit 5 | O |
| O | T/C | TC | B27 | A27 | SA4 | System Address bit 4 | O |
| ? | Buffered Address Latch Enable | BALE | B28 | A28 | SA3 | System Address bit 3 | O |
| / | Power +5V | +5V | B29 | A29 | SA2 | System Address bit 2 | O |
| O | Oscillator | OSC | B30 | A30 | SA1 | System Address bit 1 | O |
| / | Ground | GND | B31 | A31 | SA0 | System Address bit 0 | O |

### Signal Description

**CLOCK** (*System Drive*) output
The system clock is a synchronous microprocessor cycle clock.

**RESET** (*Reset Drive*) output
This signal goes high at power-up, hardware reset, or when low line-voltage occurs.

**SA0 to SA19** (*System Addresses*) input/output
The system address lines run from bit 0 through 19. They are latched onto the falling edge of BALE.

**SD0 to SD7** (*System Data bits*) Input/Output
System data bits 0 to 7.

**BALE** (*Buffered Address Latch Enable*) input
The buffered address latch enable is used in latch SA0 to SA19 on the falling edge of BALE. During DMA cycles, BALE is forced high.

**IO CHK** (*I/O Channel Check*) active low input
I/O channel check is active low signal which indicate that a parity error exists in the I/O board.

**IO RDY** (*I/O Channel Ready*) input
This signal lengthens I/O or memory cycles and should be held low with valid addresses. It can be held low for a maximum of 2.5 microseconds.

**IRQ 3 to 7, 9** (*Interrupt Requests*) input
These interrupt request signals indicate I/O service request attention. They are prioritized in the following sequences: highest IRQ 9 and lowest IRQ 3, 4, 5,6,7,8.

**IOR** (*I/O Read*) active low input/output
Instructs an I/O device to drive its data onto the data bus.

**IOW** (*I/O Write*) active low output
Instructs an I/O device to read the data off the data bus.

**SMEMR** (*System Memory Read*) output
The system memory read signal is low while the low first megabyte memory is being read.

**SMEMW** (*System Memory Write*) output
The system memory write signal is low while the low first megabyte memory is being written.

**DRQ 0 to 3** (*DMA Requests*) active high input
DMA Request channels 0 to 3 are for 8-bit data transfers. DRQ4 is used on the system board. Hold a DRQ line high until its DMA Request Acknowledge (DACK) goes active. Their priority is in the following sequences: highest DRQ 0,1,2, and 3.

**DACK 1 to 3** (*DMA Request Acknowledges*) output
These signals are used to acknowledge the corresponding signals for DRQ 0 to 3.

**AEN** (*Address Enable*) output
The address enable is high when the DMA controller drives the address bus and is low when the CPU drives the address bus.

**REFRESH** (*Refresh cycle in progress*) active low input/output
This signal indicates a refresh cycle is in progress.

**TC** (*T/C*) output

**OSC** (*Oscillator*) output
The oscillator signal is used for the color graphic card.
High-speed clock (70 ns, 14.31818 MHz), 50%duty cycle

**0WS** (*Zero Wait State*) input
The zero wait state indicates to the microprocessor that the present bus cycle can be completed without inserting any additional wait cycles.