The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination –2005
ECD 2209 – Fault Diagnosis in Electronic Circuits **(Closed Book)**

Time: 0900-1200hrs. Date: 07.04.2006

Answer any five questions.

1. (a) Consider the amplifier shown in Figure-Q1.

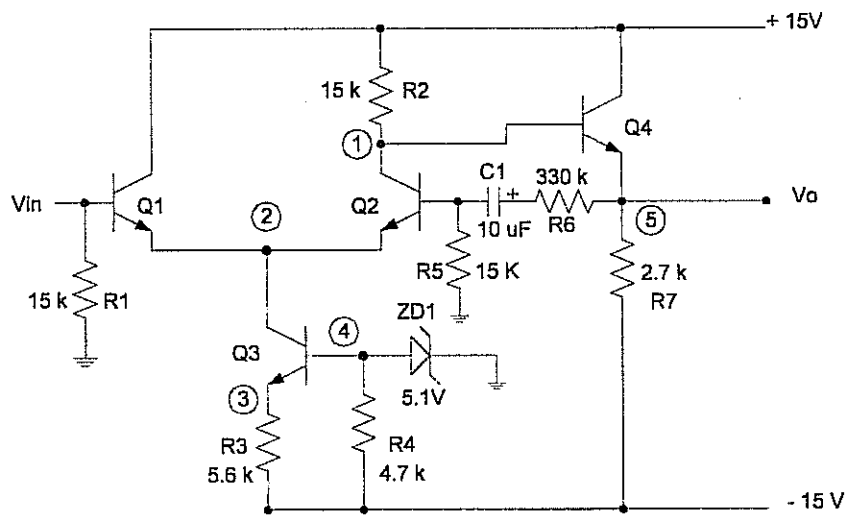

Figure - Q1

(i) The transistors Q1, Q2 are matched and the gain of Q1, Q2 and Q4 is high. Assuming the β of Q3 is 100, calculate the test point voltages at no signal. Do not assume the voltage at test point 5 as zero.

(ii) If the amplifier is working properly, sketch the output voltage if the input is a 0.5V peak to peak sine wave signal of 1 kHz. Your sketch must contain both input and output waveforms marked with the relevant voltage and time values.

(iii) Voltages of the test points measured with a DVM under fault conditions are given below. Identify the faulty component/s and the type of the fault giving reasons.

case	1	2	3	4	5
A	-0.80	-0.60	-1.60	-1.00	-1.40
B	-0.80	-0.60	-5.70	-5.10	-1.40
C	2.67	-0.60	-5.70	-5.10	-15.00
D	-9.92	-0.60	-5.70	-5.10	-10.52

2. A two-stage amplifier is shown in Figure-Q2.

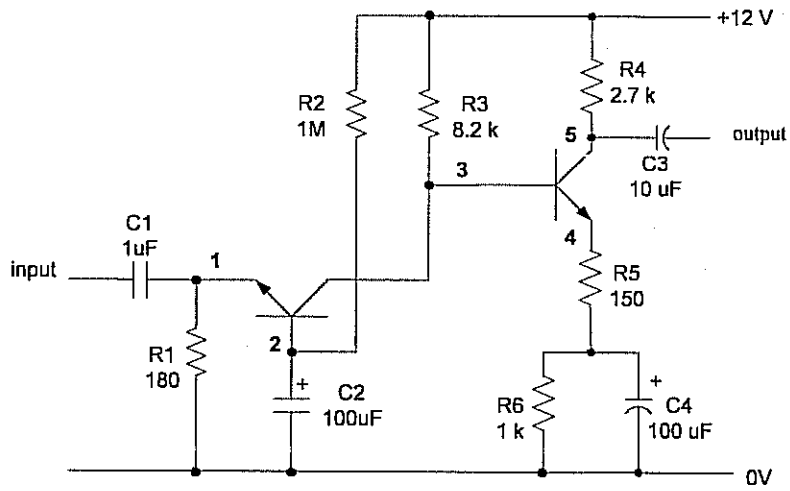

Figure - Q2

(a) If the value of β for both transistors is 100, calculate the test point voltages at no signal. Do not assume for maximum output swing.

(b) When the amplifier is given 1mV peak to peak sine wave input, the signal observed at test point-3 is 0.238V peak to peak. Calculate the amplitude of the signal voltage observed at the output. You may assume the capacitors offer negligible reactance at the signal frequency.

(c) Following voltage readings of the test points are observed from a DVM under faulty conditions. Identify the faulty component/s with fault type giving reasons. The readings are in volts unless otherwise stated.

case	1	2	3	4	5	output
A	2.1mV	0.602	4.120	3.520	3.720	no output
B	0.204	0.804	1.036	0.436	0.630	no output
C	0.204	0.804	1.220	0.620	0.822	no output
D	0.204	0.804	2.820	0	12.00	no output

3. (a) State the advantages and the disadvantages of linear regulators over switch mode regulators.

(b) A dc power supply is shown in Figure-Q3.

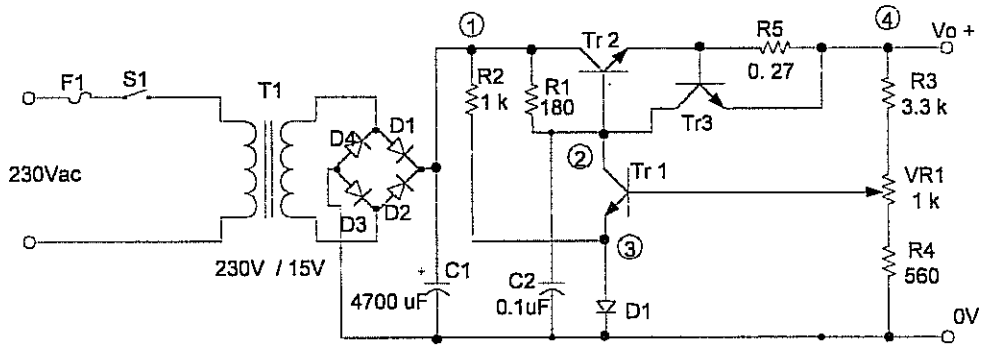

Figure-Q3

(i) Calculate the range of the output voltage.

(ii) Is it possible to use this supply for a 27W load at 9V? If not, show how you are going to modify the circuit to achieve this.

(iii) Following table shows the voltages at the test points under fault conditions. Find the faulty component/s and fault type giving reasons. Assume VR1 is set to give the maximum output.

case	1	2	3	4
A	15.00	14.80	0.60	14.20
B	15.00	6.96	0.60	6.36
C	15.00	5.81	0	5.21
D	15.00	14.80	0	14.20
E	15.00	15.00	0.60	0

4. (a) An n-channel MOSFET is tested using an analog multimeter set to x10kΩ range. Indicate the expected response in a table as shown below. Give the response as high Ω; low Ω, non-conducting or conducting.

Black Probe	Red Probe	Response
Drain	Source	
Source	Drain	
Source	Gate	
Gate	Source	
Drain	Gate	
gate	drain	

(b) A test circuit for a thyristor is shown in Figure-Q4. The data for this device is as follows.

Maximum forward blocking voltage = 100V
Maximum forward current = 2A
Maximum reverse breakdown voltage = 100V
Minimum holding voltage = 2V
Minimum holding current = 25mA
Minimum gate pulse voltage = 3V
Minimum gate pulse current = 10mA
Maximum gate voltage = 8V
Maximum gate current = 100mA

(i) Find suitable values for E_a, R_1, R_2 and R_3.
(ii) Explain how you are going to test the thyristor using this circuit.

(c) In a repair, following components are found faulty and they have to be replaced with equivalents since original part numbers are not available. State what parameters you need to consider in each of them.

Transistor, Rectifier diode, Zener diode and an inductor

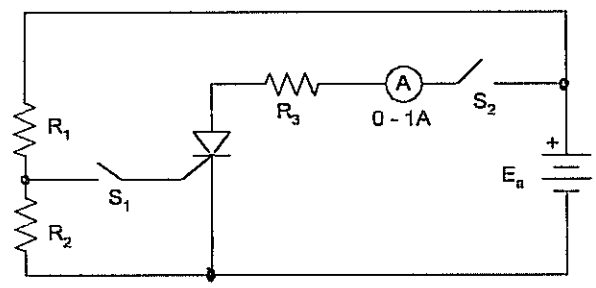

Figure – Q4

5. (a) State the use of Schmitt trigger in electronic circuits.
(b) The circuit shown in Figure-Q5 uses a Schmitt trigger with a JFET.

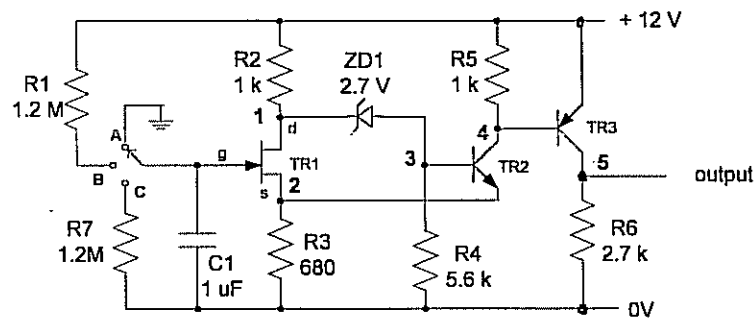

Figure-Q5

(i) Assume the FET starts to conduct when $V_{GS} > -1$ and when the FET is 'ON', its V_{DS} is 1V. Calculate the threshold voltages of V_g at which the output of the circuit will change.

(ii) Calculate the test point voltages for the two states of the output. Assume $V_{CE\,sat}$ for TR2 and TR3 is 0.2V.

(iii) The switch is initially at position A. If it is turned to position B for one second and then turned to position C, calculate the output pulse width.

(iv) Following table shows three fault cases with the measured test point voltages when the switch is at position A. State faulty component/s with fault type giving reasons.

case	1	2	3	4	5
A	10.08	6.78	7.38	2.03	0
B	6.28	3.52	4.12	11.40	11.80
C	6.54	3.24	3.84	12.00	0

6. Consider the circuit shown in Figure-Q6.

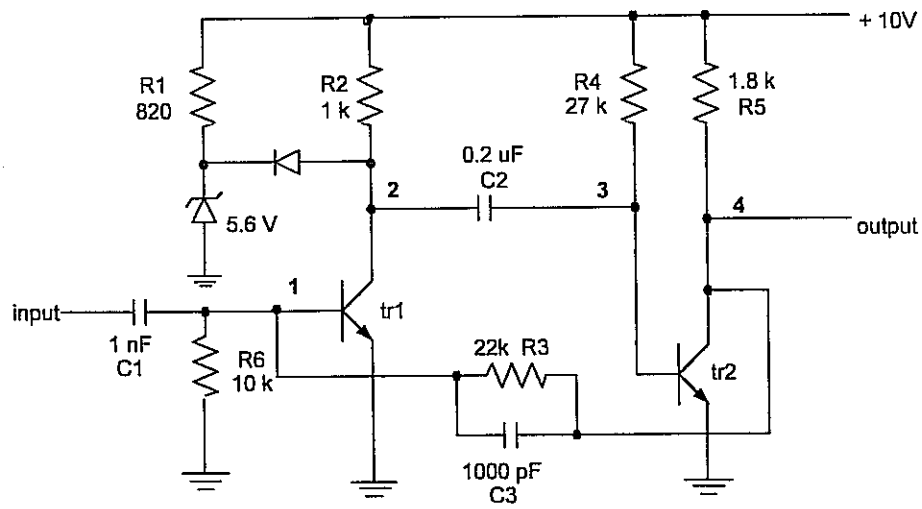

Figure-Q6

A narrow width pulse train of 250 Hz frequency and +2V height is applied to the input.

(a) Draw the waveforms at each test point to a common time scale with the input.

(b) Calculate the parameters of the output waveform.

(c) Calculate the voltages at test points when no signal is applied.

(d) The output is not available under the following fault conditions. State which component is faulty with fault type giving reasons.

case	TP1	TP2	TP3	TP4
A	0.2	6.2	0.7	0.2
B	0.6	0.2	0.7	10
C	0.2	0.6	0.7	0.2
D	0.2	0	0.7	0.2

7. Consider the logic circuit shown in Figure-Q7.

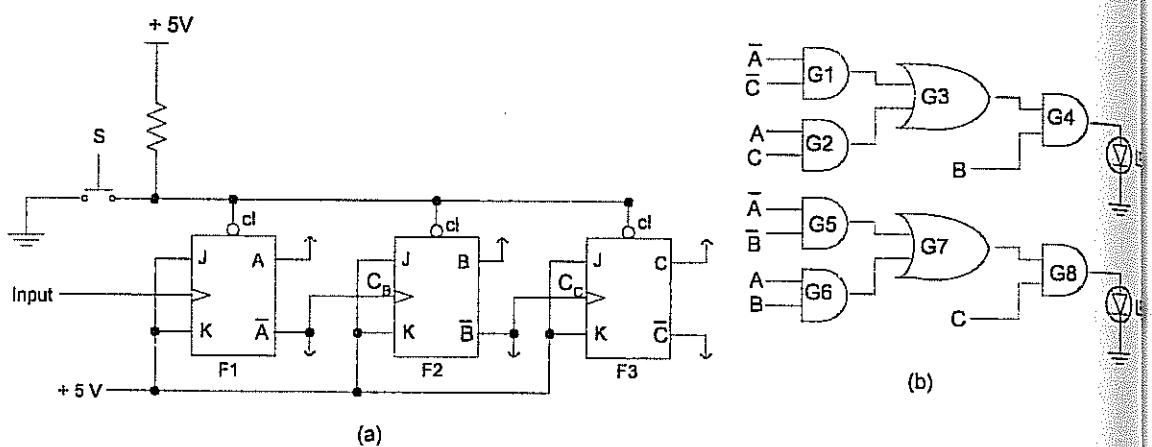

Figure-Q7

Assume the logic outputs of the circuit section(a) are connected to the logic inputs of the circuit section(b). The JK flip-flops are +ve edge trigger(triggers on the +ve edge of the clock) type.

(a) After pressing S, clock pulses are given to the input. Draw the timing diagram to show A,C_B,B,C_C and C for the first eight clock pulses. Hence tabulate the number of clock pulses with the relevant binary values of A,B and C.

(b) Tabulate the number of clock pulses with the status (ON/OFF) of the LED-1 and LED-2.

(c) Following table shows LED status with the clock pulses (after S is pressed to initialize) under faulty conditions. Identify the faulty component/s with the type of the fault. Assume the circuit connections are in good order.
LED "ON" = 1 LED "OFF' = 0

clock pulse		1	2	3	4	5	6	7	8
case A	LED-1	0	0	1	0	0	0	1	0
	LED-2	0	0	1	1	0	0	1	1
case B	LED-1	0	0	0	0	0	0	1	0
	LED-2	0	0	0	1	0	0	1	0
case C	LED-1	0	1	0	0	0	0	1	0
	LED-2	0	0	0	1	0	0	0	0

8. (a) Explain the use of logic probe and logic pulser to test the gate G1 shown in Figure – Q8 (a).

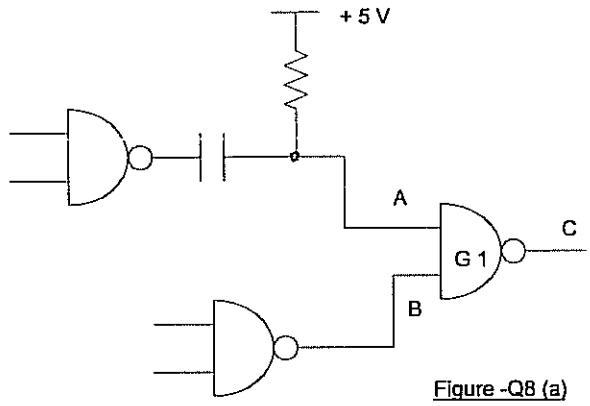

Figure -Q8 (a)

(b) Consider the logic circuit shown in Figure – Q8 (b).

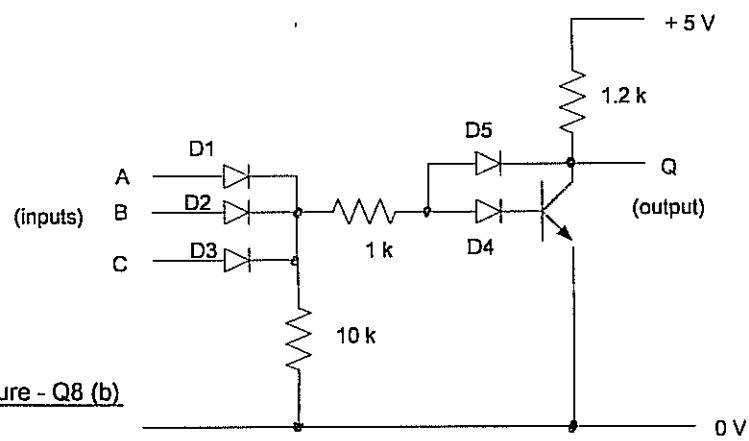

Figure - Q8 (b)

(i) Give the truth table of this circuit.
(ii) State the logic function of this circuit.
(iii) Following table shows the observations of inputs using the logic probe.

A	B	C
No light No light light	No light Light light	Light Blink Blink

Indicate the corresponding observations of the logic probe on the output Q for the following faults for each of the above input conditions.

Fault 1:- D4 short circuited
Fault 2:- D3 short circuited