The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination –2006
ECX 4230 – Fault Diagnosis in Electronic Circuits **(Closed Book)**

Time: 0930-1230 hrs. Date: 04.04.2007

Answer any five questions.

1. A differential amplifier circuit is shown in Figure-Q1.

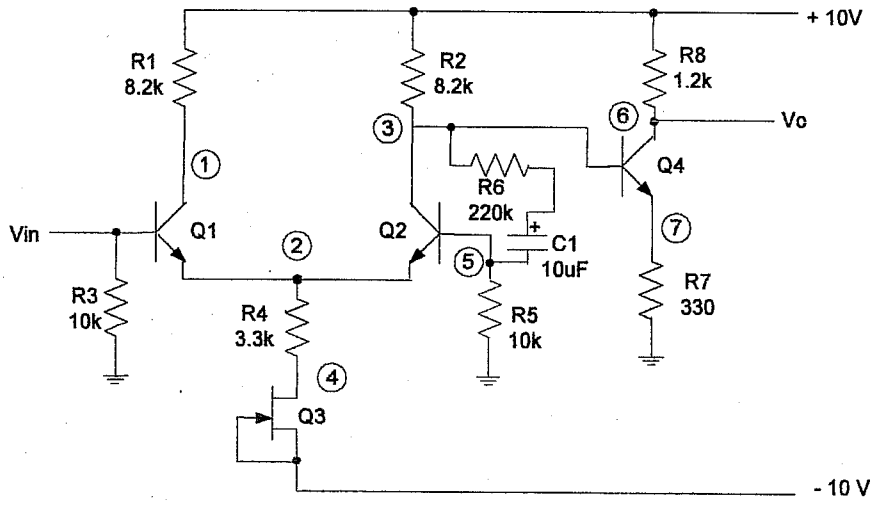

Figure - Q1

The transistors Q1, Q2 and Q4 are of high gain and Q1 and Q2 are matched. The transistor Q3 is an n-channel JFET in which $I_D = 0.125(V_{GS}-V_P)^2$, where $V_P = -4V$. You may assume usual notation.

(i) Calculate the test point voltages at no signal. (Do not assume a value for test point 6.)

(ii) A signal of 1 kHz, 40mV peak to peak is given to the input and the resulting waveforms at the test points are observed using an oscilloscope. Draw the waveforms observed at the test points 3 and 6 to a common time scale with the input for the following settings.
   (a) When the vertical amplifier of the scope is dc coupled.
   (b) When the vertical amplifier of the scope is ac coupled.

(iii) Following table shows test point voltages under fault conditions. Identify the faulty component/s with fault type giving reasons.

case	1	2	3	4	5	6	7
A	10.00	0	10.00	0	0	2.23	2.13
B	-0.50	-0.60	2.96	-7.20	0	2.46	2.36
C	1.80	-0.60	1.80	-7.20	0	1.50	1.20
D	1.80	-0.60	1.80	-7.20	0	10.00	0

2. A two-stage preamplifier circuit is shown in Figure-Q2.

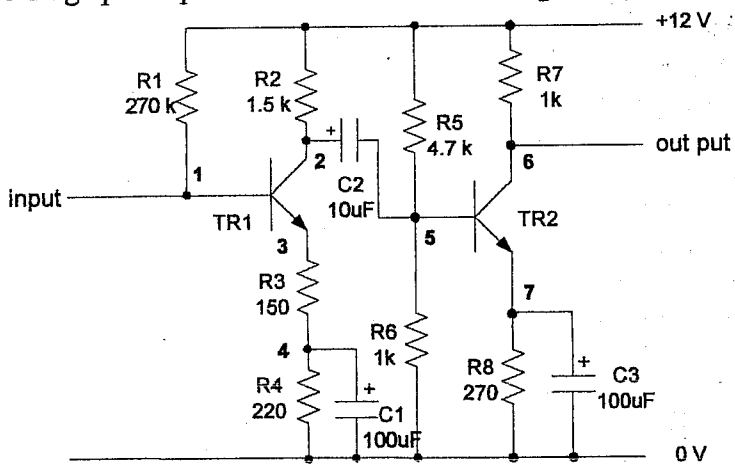

Figure-Q2

The transistors are of silicon and the current gain β of TR1 and TR2 is 75 and 50 respectively.

(a) Calculate the test point voltages at no signal. (Do not assume a value for test point 6.)

(b) When a 1 kHz sine wave is given to the input, the signal at test point 6 becomes 2V peak to peak when the signal at test point 5 is 9.7mV peak to peak. Find the amplitude and the phase of the output if the input is 2mV peak to peak.

(c) Following is a table of dc test point voltages measured by a DVM under fault conditions of the circuit. When the signal voltages are observed, the input is given a 1kHz, 2mV peak to peak sine wave test signal. Identify the faulty component/s stating the fault type and reasons to justify your answer.

case	1	2	3	4	5	6	7	other
A	1.69	7.70	1.09	0.65	2.02	6.85	1.42	8.12mVp-p at 5 & 1.67Vp-p at 6
B	1.69	7.70	1.09	0.65	3.11	2.71	2.51	no output
C	1.69	7.70	1.09	0.65	0.97	12.00	0.37	no output
D	6.33	9.64	5.61	0.35	2.02	6.85	1.42	0.9mVp-p at 5 & 185mVp-p at 6

3. The circuit shown in Figure-Q3(a) is a dc-dc switching regulator. In this circuit, U1 is a comparator and RG is a ramp generator. Waveforms observed at 5 for three values of voltages at 3 are shown with the ramp generator out put at 2 in Figure-Q3(b).

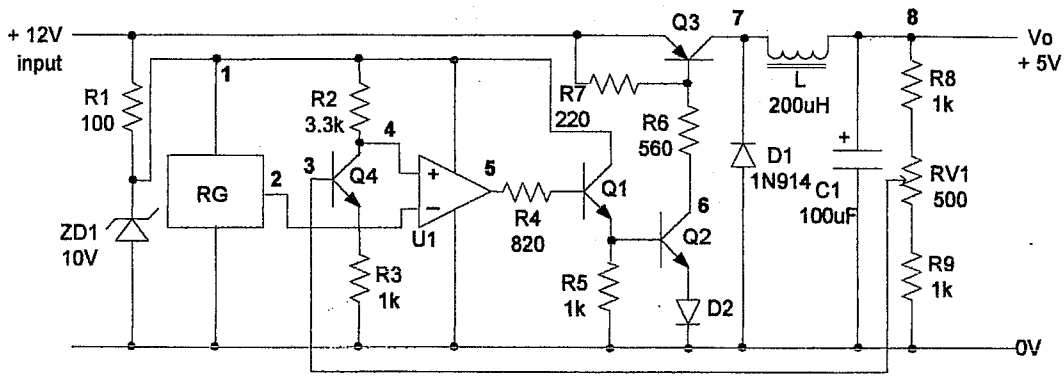

Figure-Q3 (a)

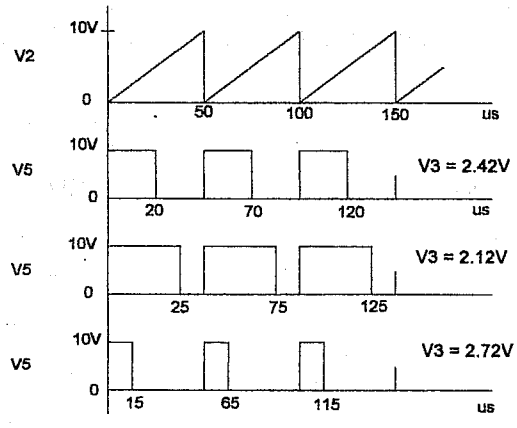

Figure-Q3(b)

(i) State the role of the following components in relation to the operation of the circuit.
ZD1, Q2, Q3, Q4, L, D1 and C1

(ii) State briefly how this circuit regulates the output voltage when the load current is varied.

(iii) Following table shows the observations on test points under faulty conditions. Determine the faulty component/s with the type of the fault stating reasons. Fault free operating values of some of the test points are, TP3 = 2.42V, TP4 = 4V, TP5 = 20 µs pulse width, TP8 = 5V.

case	1	2	3	4	5	6	7	8
A	10.00	ramp	1.81	6.00	30µs	pulse	pulse	8.00
B	10.00	ramp	3.00	2.43	12.2µs	0.60	11.80	11.80
C	10.00	ramp	0	10.00	10.00	0.70	11.80	0
D	10.00	ramp	3.00	2.43	10.00	0.70	11.80	1.80

Note that all the values are dc voltages unless otherwise stated. Pulse widths measured are given in µs.

4. A circuit used to process an analog signal is shown in Figure-Q4.

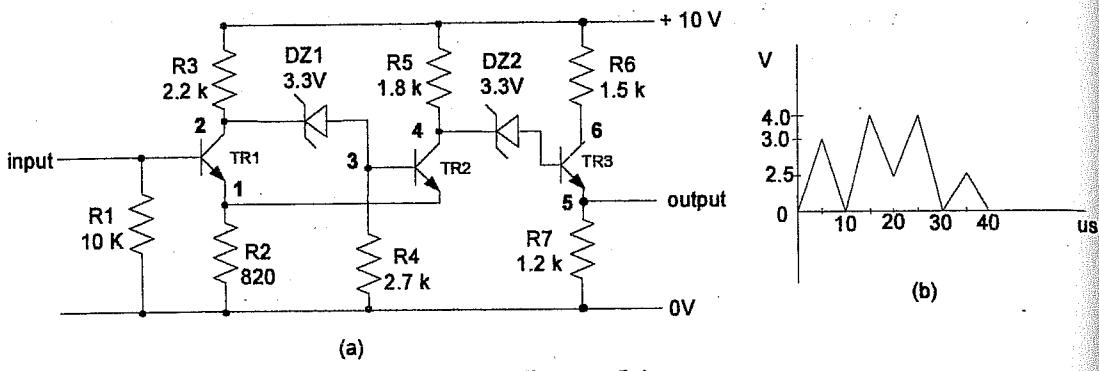

Figure - Q4

(a) Calculate the input voltages at which the state of the output is changed.
(b) Calculate the test point voltages for an input voltage of zero and 5V.
(c) Sketch the output signal if the signal shown in Figure-Q4(b) is given to the input.
(d) Under fault conditions, this circuit is tested giving dc input voltages. The resulting test point voltages measured with a DVM are shown below. Identify the faulty component/s in each case giving the fault type with reasons.

case	input	1	2	3	4	5	6
A	4.00	3.40	3.50	0.10	10.00	0	10.00
B	5.00	3.09	6.99	3.68	8.36	5.00	5.01
C	2.00	3.09	6.99	3.69	8.35	5.00	5.01
D	2.00	0	6.99	3.68	8.35	5.00	5.01

5. Consider the circuit shown in Figure-Q5.

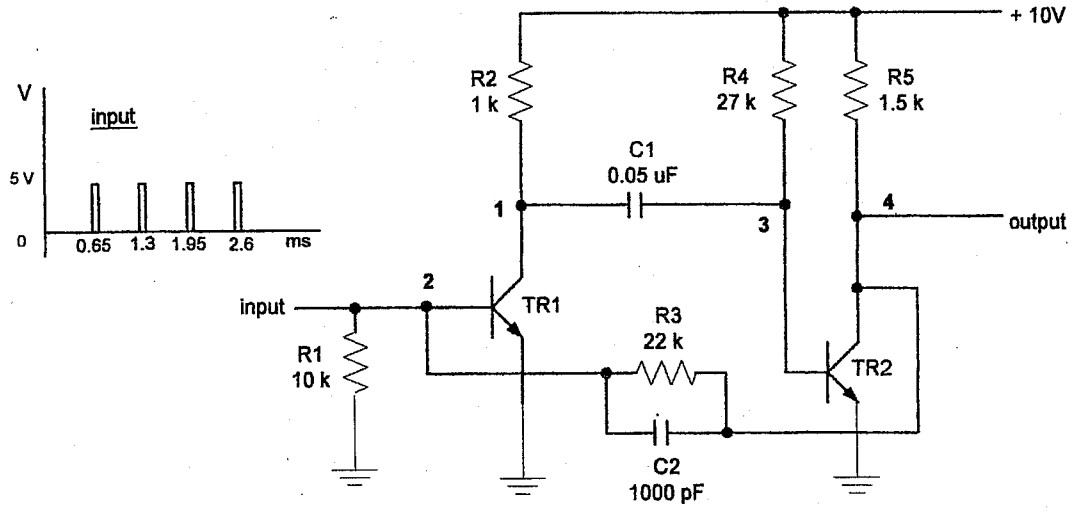

Figure-Q5

(a) Find the voltages at the test points when no input signal is applied. What are the collector currents of the transistors in this case?

(b) The narrow width pulse train shown in the figure is applied to the input. Draw the resulting waveforms at each test point in a timing diagram marking important voltages and time values. Show the calculations of these values clearly.

(c) In each of the following cases, the circuit fails to produce the expected output when the pulse train is applied. State which component/s is faulty giving the fault type with reasons. Note that the values shown are the dc voltages measured at the test points.

case	1	2	3	4	comments
A	10.00	0.01	0.60	0.01	no output, narrow – ve pules at 1
B	0.01	0.60	10.00	9.40	no output
C	0.01	0.60	0.60	9.40	no output
D	10.00	0.01	0.60	0.01	frequency of the output is 512.8Hz

6. The circuit shown in Figure-Q6 is a Wien bridge oscillator.

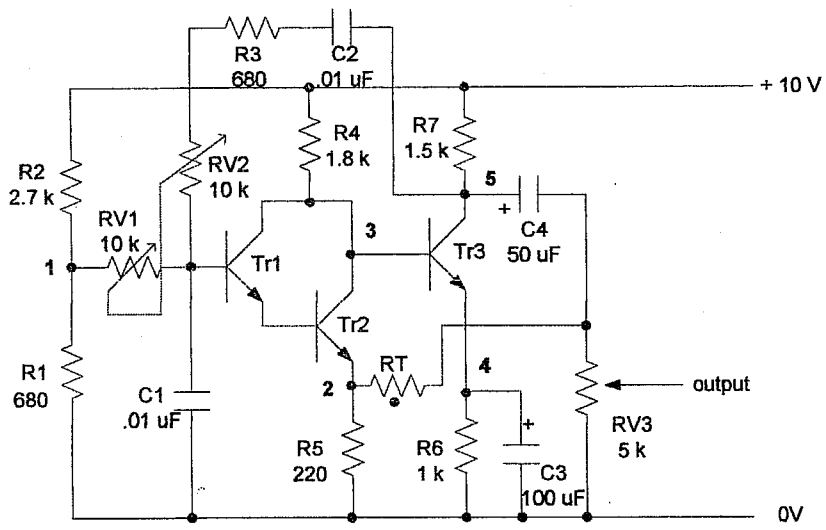

Figure-Q6

(a) Briefly explain the principle of operation of this circuit.

(b) Estimate the operating frequency range of the oscillator.

(c) Calculate the dc voltages at the test points.

(d) Following table shows the dc voltages at the test points under fault conditions. Identify the faulty component/s with fault type indicating reasons to support your answers.

case	1	2	3	4	5	comments
A	2.01	0	9.68	9.08	9.20	no output
B	2.01	0.81	3.38	2.78	5.83	square wave
C	0	0	9.68	9.08	9.20	no output
D	2.01	0.81	3.38	2.78	10.00	no output

7. (a) You are required to modify a driver PCB of an equipment by implementing an additional transistor relay driver circuit. Draw a circuit of a suitable transistor relay driver and derive the specifications of the components required. State the function of each component in the circuit. Following data is available to you.

Power supply = 12V Resistance of the relay = 10Ω

Input driving signal = 5V@ 40mA V_{CEsat} = 0.3V

(b) If you make a PCB of this circuit, explain a way to check the transistor and the relay without de-soldering.

(d) Consider the waveform shaping circuit shown in Figure-Q7(a).

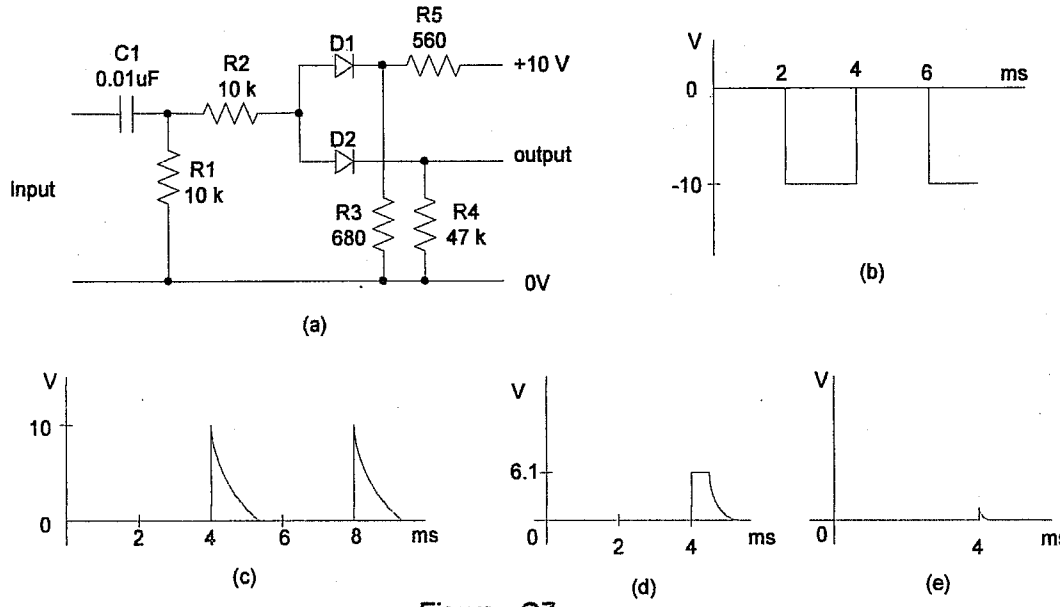

Figure - Q7

(i) If the signal shown in Figure-Q7(b) is applied to the input, sketch the resulting output signal.

(ii) Under three different fault conditions, the output signals obtained are shown in Figure-Q7(c) to Figure-Q7(e). State the components that are faulty in each case with fault type.

8. (a) Explain the use of logic probe, logic pulser and current tracer.
(b) What are the limitations of a logic probe?
(c) Consider the logic circuit shown in Figure-Q8.

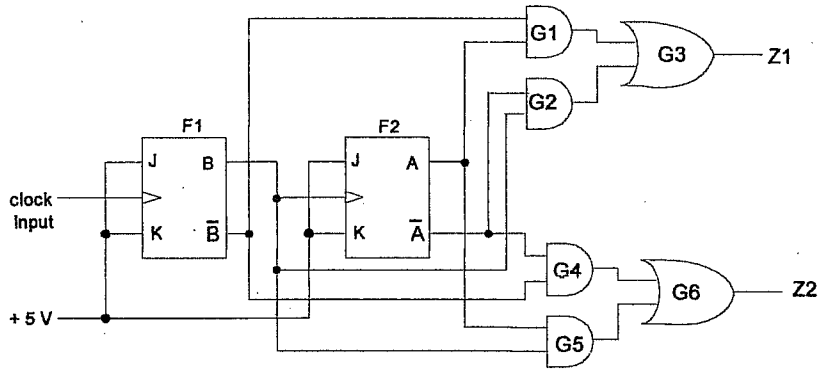

Figure-Q8

(i) The JK flip-flops are of (–)ve edge trigger type and the clock pulses are given after resetting the flip-flops. Draw a timing diagram to show the clock and the signals at A and B.

(ii) Tabulate the number of clock pulses with A_t, B_t, A_{t+1}, B_{t+1}, Z1 and Z2. Note that 't' and 't+1' are the instances before and after the clock pulse respectively.

(iii) Following table shows the logic status of Z1 and Z2 observed by a logic probe with the clock pulses under fault conditions. Assume the flip-flops are cleared before applying the clock pulses. Identify the faulty component/s with the type of fault.
In case C, state how you are going to use the logic probe to analyze further the conclusions obtained from the observations given.

clock pulse		**1**	**2**	**3**	**4**
case A	Z1	1	0	1	0
	Z2	0	1	0	1
case B	Z1	0	1	0	0
	Z2	0	0	1	1
case C	Z1	1	1	0	0
	Z2	1	1	1	1