The Open University of Sri Lanka
Department of Electrical and Computer Engineering
Final Examination –2006
ECX 3230 – Electronics **(Closed Book)**

Date: 22.03.2007 Time: 0930-1230 hrs.

Answer any five questions.

1. (a) If the collector current I_C of a transistor is given by $I_C = \beta I_B + (1+\beta) I_{CBO}$, find an expression for the stability factor of the collector current with respect to I_{CBO}.

   (b) Draw the 'fixed bias' and 'self bias' schemes for a common emitter transistor amplifier and comment on their relative stability.

   (c) The circuit shown in Figure-Q1 is a common base transistor amplifier. The current gain β of the transistor is 50.

   (i) Calculate the I_B, I_C, V_B, V_C and V_E at no signal.

   (ii) Calculate the stability factor of the circuit.

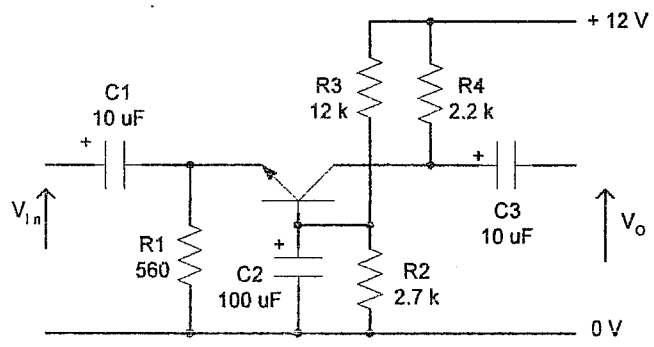


Figure - Q1

2. (a) Draw a sketch to show $I_D - V_{GS}$ characteristics for an n-channel enhancement type MOSFET. Name the regions of operation and state the expressions for the drain current in each region.

   (b) An amplifier using an n-channel enhancement type MOSFET is shown in Figure-Q2. The MOSFET has a threshold voltage of 4V and conducts a 10 mA drain current when the gate-source voltage is 6V.

   (i) This circuit shows a good stability of the bias point. Explain briefly how this is achieved.

   (ii) Calculate V_D, V_{GS}, V_S and I_D at no signal.

   (iii) Calculate the trance conductance of the device under these operating conditions.

   (iv) Calculate the voltage gain at each output for mid-band frequencies. You may assume that the reactance of the capacitors is negligible at signal frequencies. Prove any formula you use.

   (v) Find the input impedance of the amplifier.

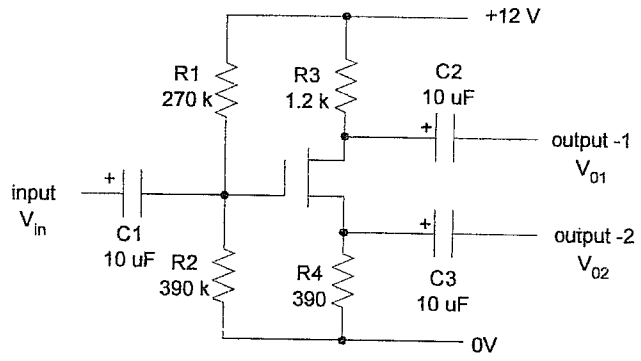


Figure -Q2

3. A dc power supply circuit is shown in Figure-Q3.

(a) Identify the configuration of this rectification. What is the other configuration used for rectification? Show it in a diagram.

(b) Sketch the waveform of the voltage V_A with V_S marking important voltage and time values. Assume that each rectifier diode has a nominal forward drop of 0.6V. State the current flow path for each half cycle of V_S using the symbols A, B, ... etc in correct sequence.

(c) If V_{DC} is the dc voltage across the load R_L, show that $V_{DC} = \dfrac{\sqrt{2}\,V_S - 1.2}{1 + \dfrac{T}{4CR_L}}$

where, T is the period of the ac input to the transformer.

(d) If the load resistance is 10Ω, calculate the value of the capacitor to have 1V peak-peak ripple at the output. What is the value of V_{DC} in this case?

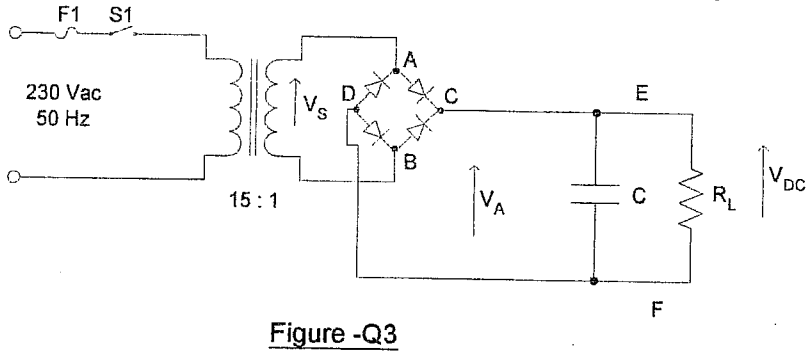


Figure -Q3

4. (a) Compare the input impedance, output impedance, voltage gain and current gain of common emitter, common collector and common base amplifiers. Give your answer using a table.

(b) A common base amplifier is shown in Figure-Q4.

(i) Draw the high frequency equivalent circuit using the h-parameters h_{ie} and h_{fe} for the transistor. You may neglect h_{re} and h_{oe}.

(ii) Using the circuit obtained in (i) above, derive expressions for the voltage gain $\dfrac{V_o}{V_s}$, the current gain $\dfrac{I_o}{I_1}$, and the input impedance Z_i for mid-band frequencies.

(iii) Calculate the values for the quantities in (ii) above.

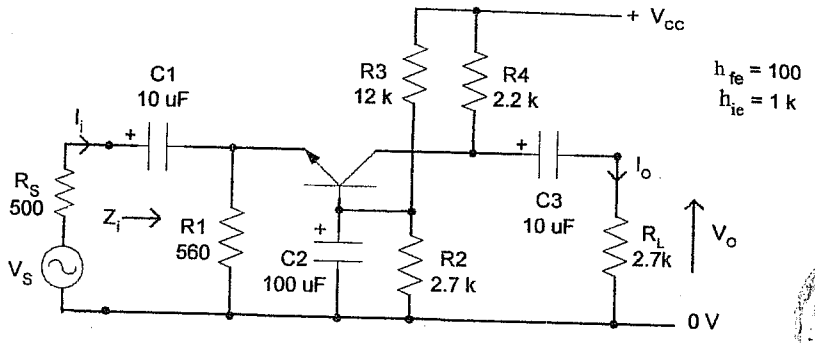


Figure - Q4

5. (a) At time t = 0, a step voltage E_0 is given to the circuit shown in Figure-Q5(a). Assume the capacitor is fully discharged before applying the step voltage.

(i) Draw a sketch to show V_C against time.

(ii) Define rise time and show it on your sketch.

(iii) Derive a formula for the rise time in terms of the time constant of the circuit.

(b) The circuit in Figure-Q5(b) is given V_{in}, the ±5V square waveform shown. Sketch the waveform V_0 with time marking the important voltage and time values. Show clearly how you obtained these values.

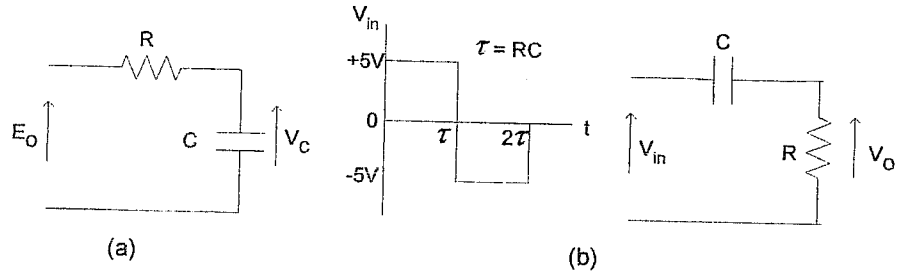


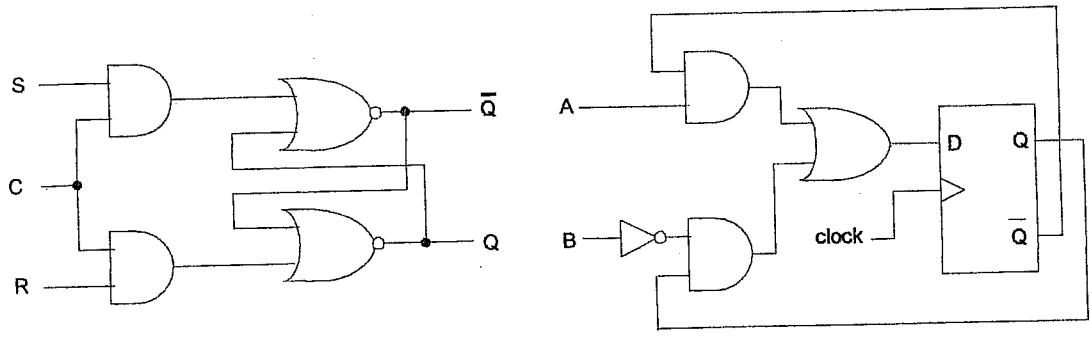
Figure -Q5

6. (a) The circuit of Figure-Q6(a) is a gated SR latch. Write the truth table indicating S, R, Q_t, $\overline{Q_t}$, Q_{t+1} and $\overline{Q_{t+1}}$ for the circuit when the clock is high. Note that the 't' denotes the instant when the clock is zero and 't+1' denotes the instant after the clock becomes high.

(b) Show how this SR latch can be used to form a D flip-flop and give its truth table.

(c) The D flip-flop formed in (b) with combinational logic is used as shown in the Figure-Q6(b). Derive the truth table for this circuit and hence identify the operation of the circuit. Explain whether the circuit is stable for all input combinations and if it is not, suggest a way to overcome that.

(d) Suggest a way to use the final circuit in (c) as a divide by two frequency divider.



(a) (b)

Figure -Q6

7. (a) Obtain the logic function of the circuit shown in Figure-Q7, in sum of products form and derive the truth table.

(b) Find the minimized solution of the following function in sum of products form using the Karnaugh's map.
$F = \Sigma\ 1,3,4,6,7,9,11,12,14$

(c) If 'A' is a three bit number, design a logic circuit to convert 'A' to its 2's complement form. Implement your circuit with NAND gates. Show the steps of your design clearly.

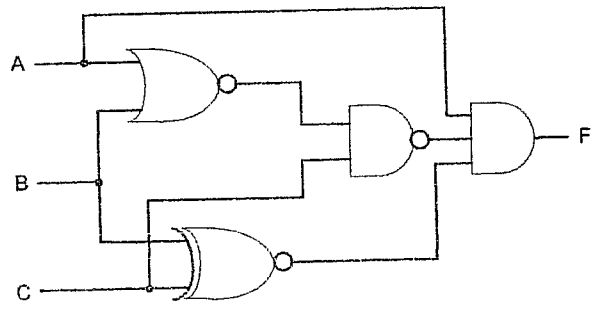


Figure -Q7

8. Consider the circuit shown in Figure-Q8. Assume the transistors are of high gain type and $V_{CE(sat)} = 0$.

(a) Calculate the voltages at the base and the collector of each transistor when there is no input signal applied for a long time. What is the collector current of each transistor?

(b) When the pulse shown is applied to the input,

(i) Show the waveform at X giving the approximate amplitude.

(ii) What are the changes that will take place in the operating state of TR1 and TR2?

(iii) Just after applying the pulse, what are the collector and base voltages of TR1 and TR2?

(iv) Derive an expression for the base voltage of TR2.

(v) After application of the pulse, calculate the time interval for which the base of TR2 is less than 0.6V.

(vi) Draw a sketch of the voltages at X, at the base and the collector of each transistor to a common time scale with the input pulse.

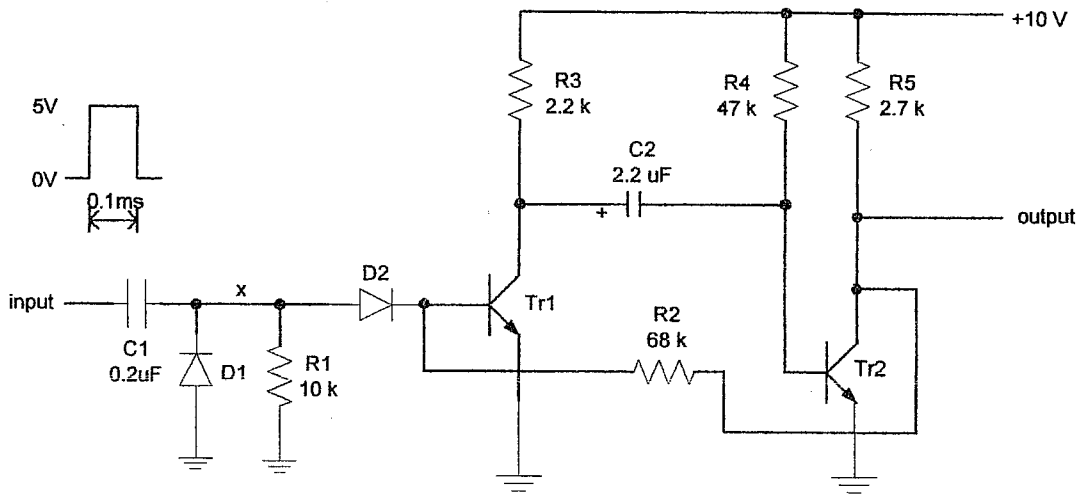

+10 V
R3
2.2 k
R4
47 k
R5
2.7 k
5V
0V
0.1ms
C2
2.2 uF
output
input
x
D2
Tr1
R2
68 k
C1
0.2uF
D1
R1
10 k
Tr2

Figure -Q8